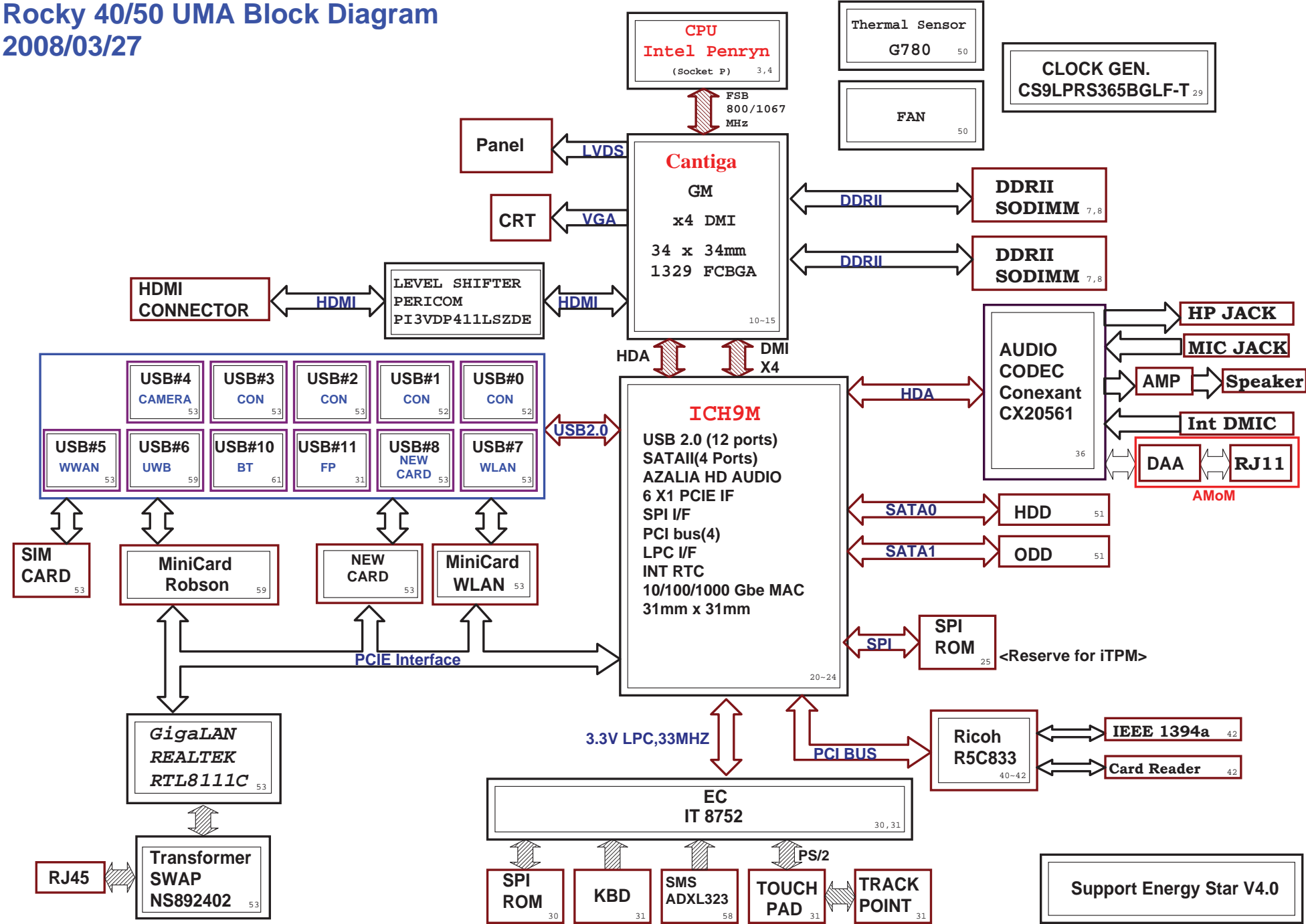


Rocky 40/50 UMA Block Diagram  
2008/03/27



## Rocky 40/50 Schematic Index

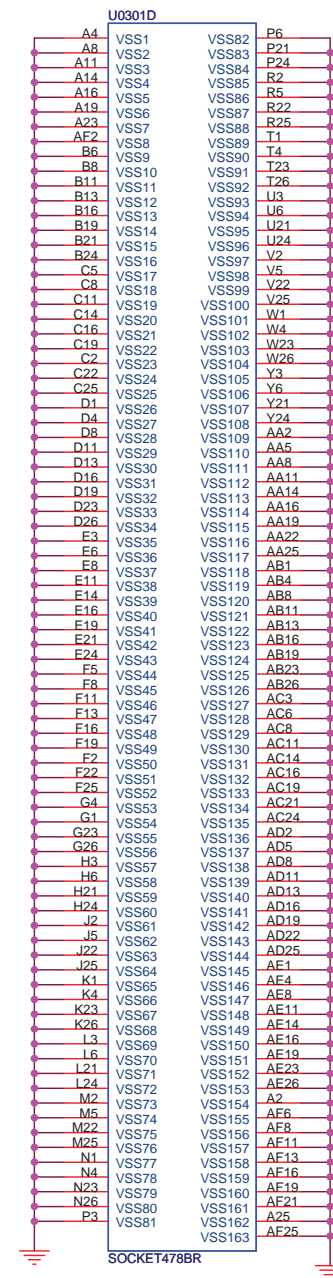
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42	IEEE1394A & 4 IN1 CON
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85	PWR_VGA_CORE & 1.1V
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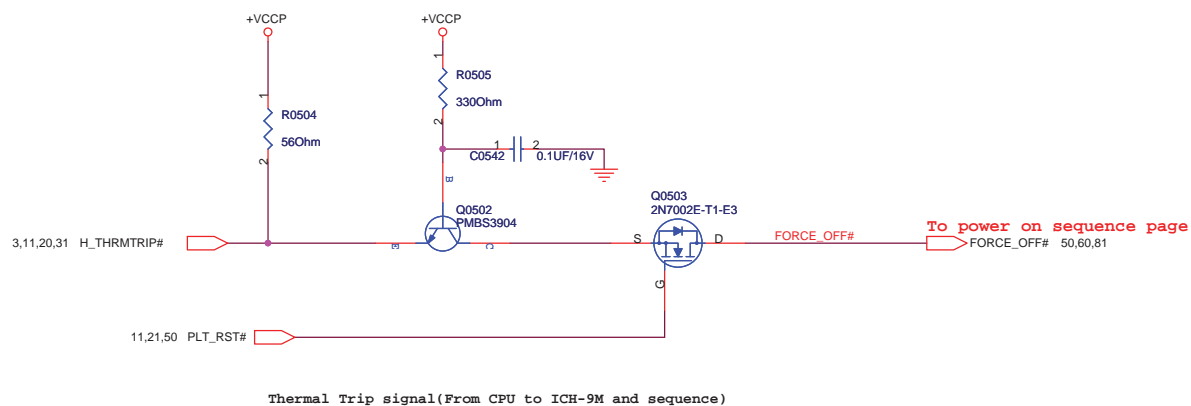
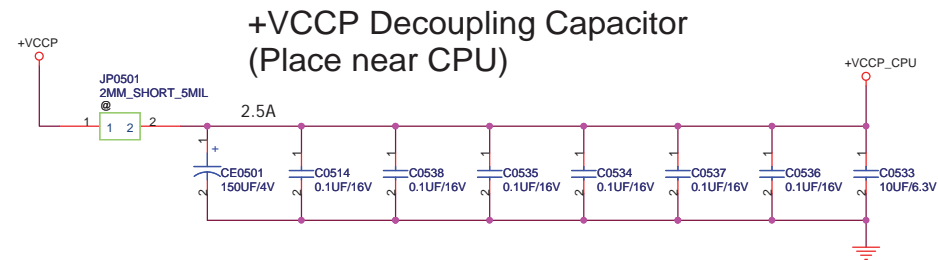
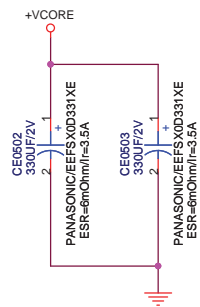
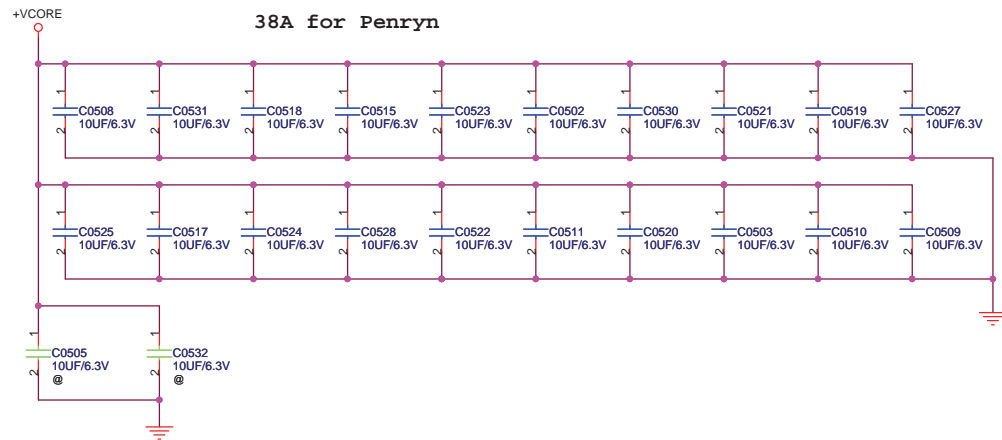
ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO		+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPO	GPIO36	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	GPO	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDCP_EEPROM_PROTECT#	+3VS
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

[illegible]









D

C

B

A

D

C

B

A

<http://hobi-elektronika.net>

PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	6	of 94



SMBus Slave Address:A0H

temp\_5886\_t101  
(12G025M22000LV with 12G025C2200WLV  
co-lay symbol)

SMBus Slave Address: A0H

Place near SO-DIMM\_0

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

VREF -> 10/10 mils





SO-DIMM 0 is placed nearer the  
GMCH than SO-DIMM 1

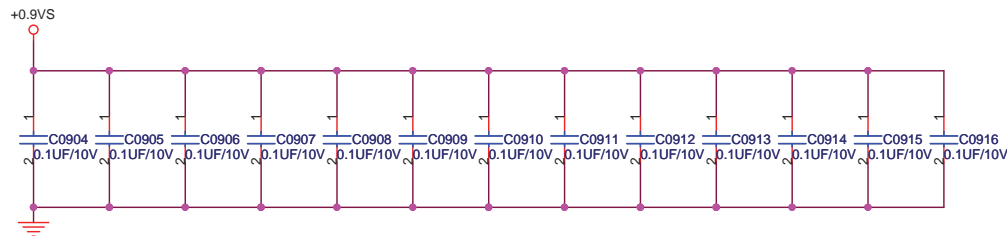
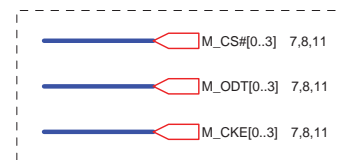
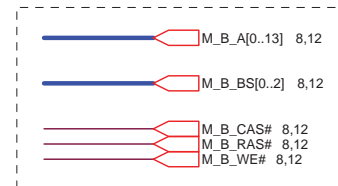
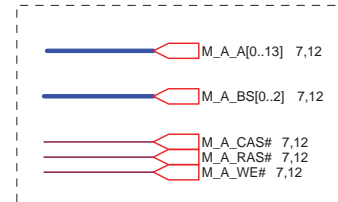
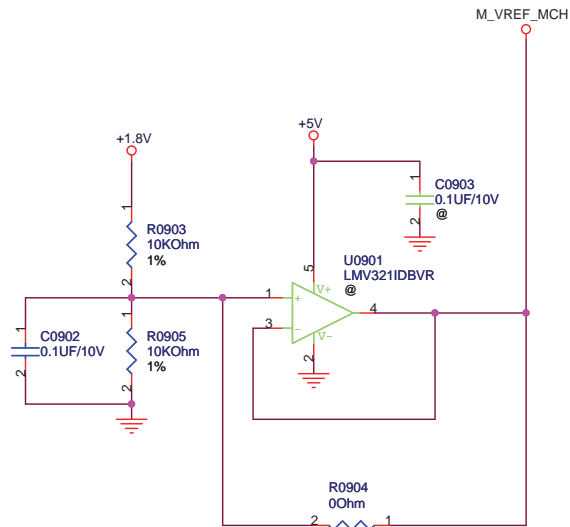
Layout Note: Place these Caps near SO DIMM 0

PLACE NEAR SO-DIMM\_0 / SO-DIMM\_1

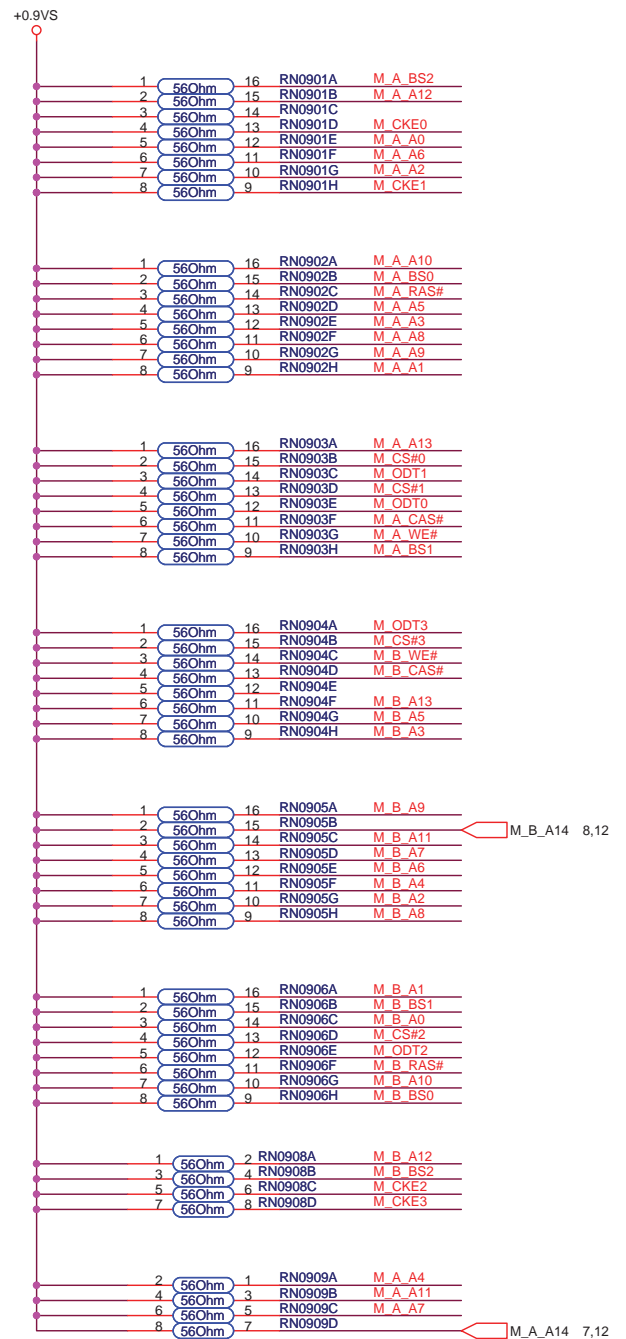
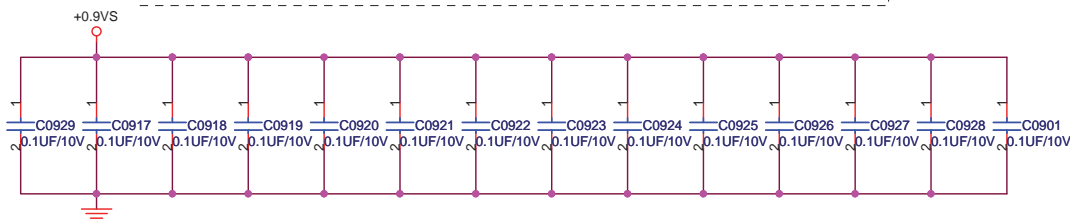


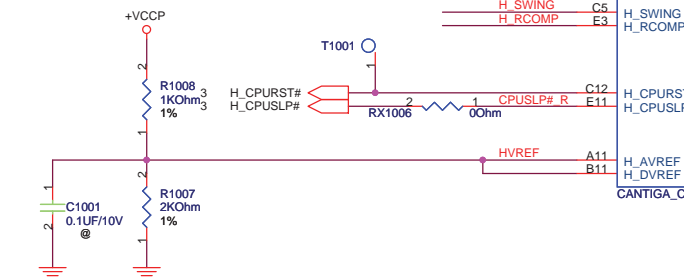
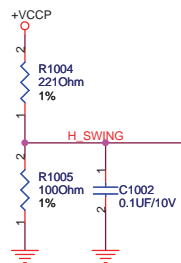
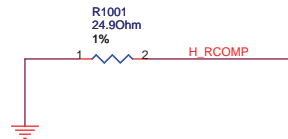


+5V  +5V 44,56,57,91  
 +1.8V  +1.8V 7,8,11,13,83,91  
 M\_VREF\_MCH  M\_VREF\_MCH 7,8,11  
 +0.9VS  +0.9VS 83

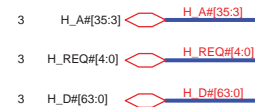
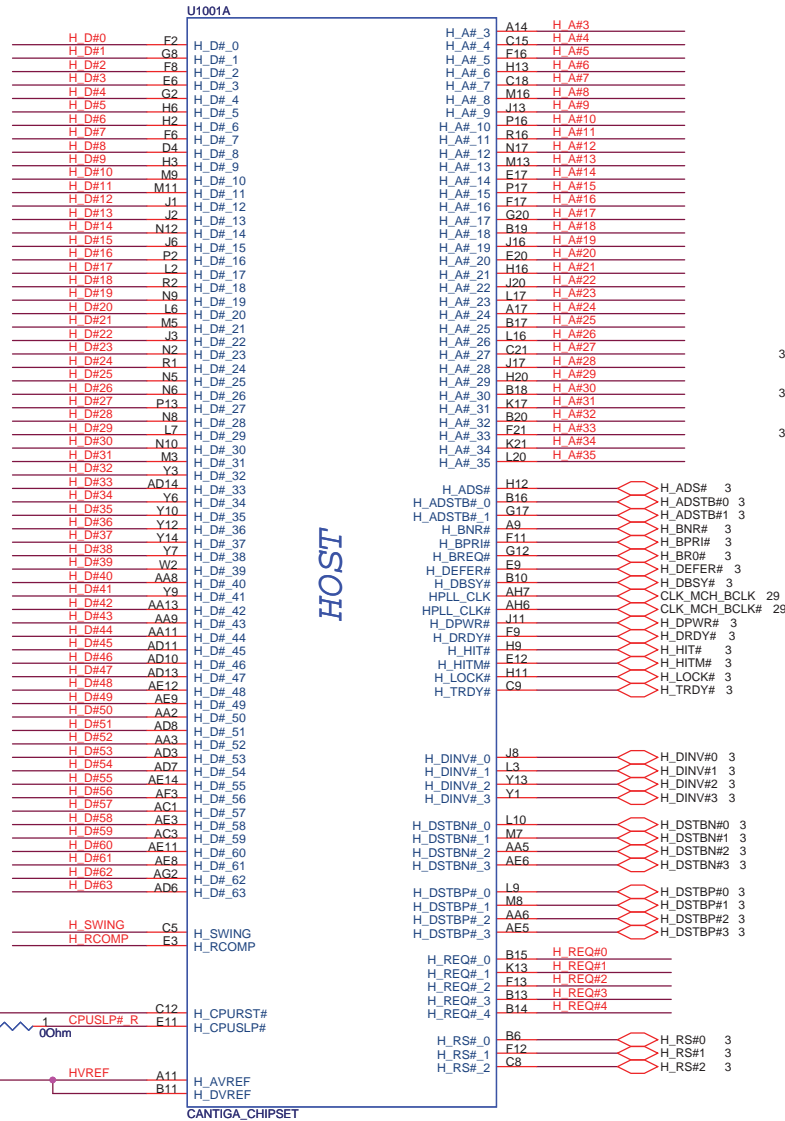


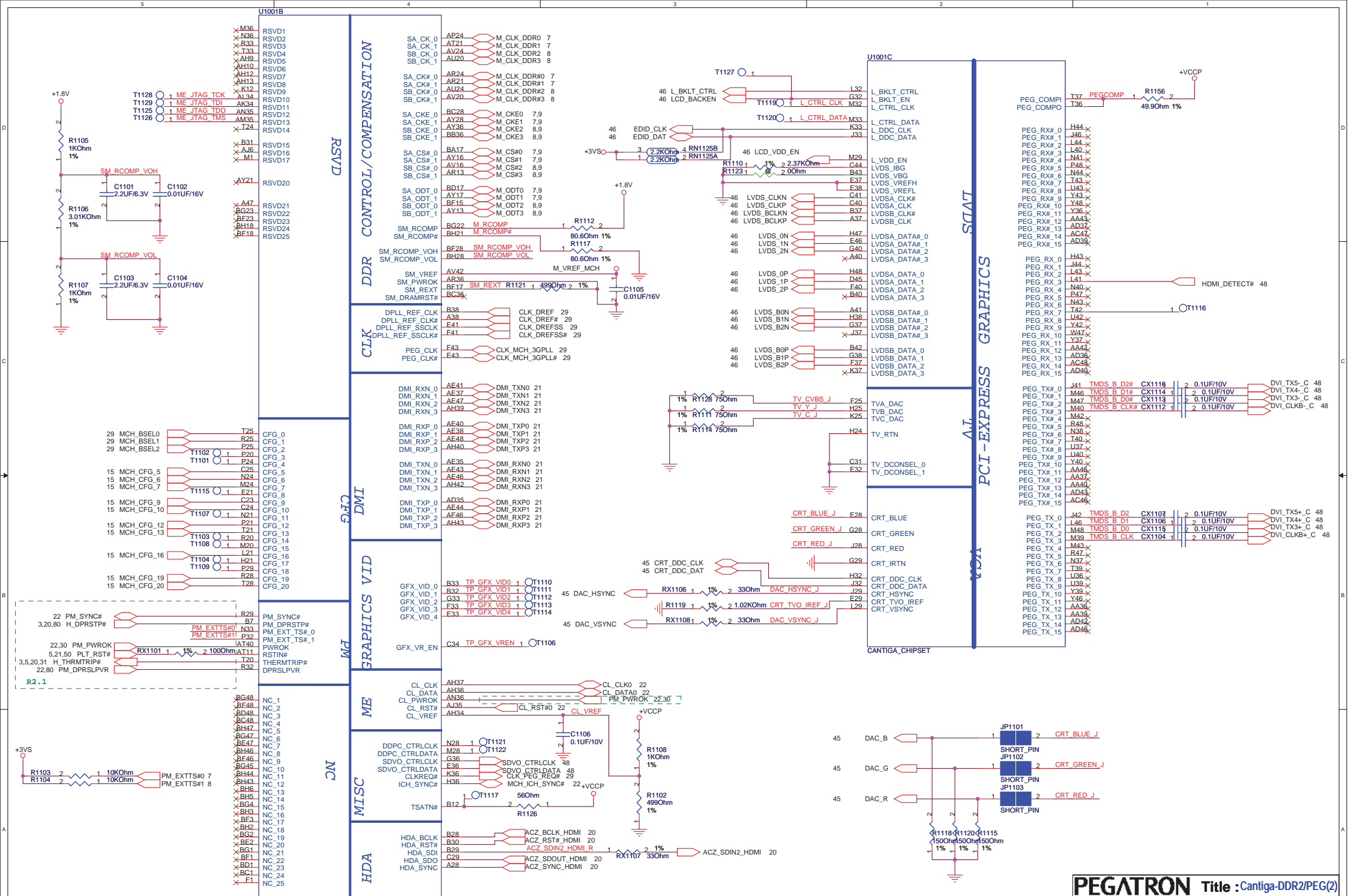
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





CAP 0.1U within 100 mils from GMCH





7 M\_A\_DQ[0:63]

U1001D  
M A DQ0 AJ38  
M A DQ1 AJ41  
M A DQ2 AN38  
M A DQ3 AM38  
M A DQ4 AJ38  
M A DQ5 AJ40  
M A DQ6 AM44  
M A DQ7 AM42  
M A DQ8 AN43  
M A DQ9 AN44  
M A DQ10 AU40  
M A DQ11 AT38  
M A DQ12 AN41  
M A DQ13 AN39  
M A DQ14 AU44  
M A DQ15 AU42  
M A DQ16 AV39  
M A DQ17 AY44  
M A DQ18 BA40  
M A DQ19 BD43  
M A DQ20 AV41  
M A DQ21 AY43  
M A DQ22 BB41  
M A DQ23 BC40  
M A DQ24 AY37  
M A DQ25 BD38  
M A DQ26 AV37  
M A DQ27 AT36  
M A DQ28 AY38  
M A DQ29 BB38  
M A DQ30 AV36  
M A DQ31 AW36  
M A DQ32 BD13  
M A DQ33 AU11  
M A DQ34 BC11  
M A DQ35 BA12  
M A DQ36 AU13  
M A DQ37 AV13  
M A DQ38 BD12  
M A DQ39 BC12  
M A DQ40 BB9  
M A DQ41 BA9  
M A DQ42 AU10  
M A DQ43 AV9  
M A DQ44 BA11  
M A DQ45 BD9  
M A DQ46 AY8  
M A DQ47 BA6  
M A DQ48 AV5  
M A DQ49 AV7  
M A DQ50 AT9  
M A DQ51 AN8  
M A DQ52 AU5  
M A DQ53 AU6  
M A DQ54 AT5  
M A DQ55 AN10  
M A DQ56 AM11  
M A DQ57 AM5  
M A DQ58 AJ9  
M A DQ59 AJ8  
M A DQ60 AN12  
M A DQ61 AM13  
M A DQ62 AJ11  
M A DQ63 AJ12

DDR SYSTEM MEMORY A

SA\_BS\_0  
SA\_BS\_1  
SA\_BS\_2  
SA\_RAS#  
SA\_CAS#  
SA\_WE#  
SA\_DM\_0  
SA\_DM\_1  
SA\_DM\_2  
SA\_DM\_3  
SA\_DM\_4  
SA\_DM\_5  
SA\_DM\_6  
SA\_DM\_7  
SA\_DQS\_0  
SA\_DQS\_1  
SA\_DQS\_2  
SA\_DQS\_3  
SA\_DQS\_4  
SA\_DQS\_5  
SA\_DQS\_6  
SA\_DQS\_7  
SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

BD21 M\_A\_BS0 7,9  
BG18 M\_A\_BS1 7,9  
AT25 M\_A\_BS2 7,9  
BB20 M\_A\_RAS# 7,9  
BD20 M\_A\_CAS# 7,9  
AY20 M\_A\_WE# 7,9  
AM37 M\_A\_DM0  
AT41 M\_A\_DM1  
AY41 M\_A\_DM2  
AU39 M\_A\_DM3  
BB12 M\_A\_DM4  
AY6 M\_A\_DM5  
AT7 M\_A\_DM6  
AJ5 M\_A\_DM7  
AJ44 M\_A\_DQS0  
AT44 M\_A\_DQS1  
BA43 M\_A\_DQS2  
BC37 M\_A\_DQS3  
AW12 M\_A\_DQS4  
BC8 M\_A\_DQS5  
AU8 M\_A\_DQS6  
AM7 M\_A\_DQS7  
AJ43 M\_A\_DQS#0  
AT43 M\_A\_DQS#1  
BA44 M\_A\_DQS#2  
BD37 M\_A\_DQS#3  
AY12 M\_A\_DQS#4  
BD8 M\_A\_DQS#5  
AU9 M\_A\_DQS#6  
AM8 M\_A\_DQS#7  
BA21 M\_A\_A0  
BC24 M\_A\_A1  
BG24 M\_A\_A2  
BH24 M\_A\_A3  
BG25 M\_A\_A4  
BA24 M\_A\_A5  
BD24 M\_A\_A6  
BG27 M\_A\_A7  
BF25 M\_A\_A8  
AW24 M\_A\_A9  
BC21 M\_A\_A10  
BG26 M\_A\_A11  
BH26 M\_A\_A12  
BH17 M\_A\_A13  
AY25 M\_A\_A14

8 M\_B\_DQ[0:63]

U1001E  
M B DQ0 AK47  
M B DQ1 AH46  
M B DQ2 AP47  
M B DQ3 AP46  
M B DQ4 AJ46  
M B DQ5 AJ48  
M B DQ6 AM48  
M B DQ7 AP48  
M B DQ8 AU47  
M B DQ9 AU46  
M B DQ10 BA49  
M B DQ11 AY48  
M B DQ12 AT47  
M B DQ13 AC47  
M B DQ14 BM43  
M B DQ15 BC47  
M B DQ16 BC46  
M B DQ17 BC44  
M B DQ18 BG43  
M B DQ19 BF43  
M B DQ20 BE45  
M B DQ21 BC41  
M B DQ22 BF40  
M B DQ23 BF40  
M B DQ24 BG38  
M B DQ25 BF38  
M B DQ26 BH35  
M B DQ27 BG35  
M B DQ28 BH40  
M B DQ29 BG39  
M B DQ30 BG34  
M B DQ31 BH34  
M B DQ32 BH14  
M B DQ33 BG12  
M B DQ34 BH11  
M B DQ35 BG8  
M B DQ36 BH12  
M B DQ37 BF11  
M B DQ38 BF8  
M B DQ39 BG7  
M B DQ40 BC5  
M B DQ41 BC6  
M B DQ42 AY3  
M B DQ43 AY1  
M B DQ44 BF6  
M B DQ45 BF5  
M B DQ46 BA1  
M B DQ47 BD3  
M B DQ48 AV2  
M B DQ49 AU3  
M B DQ50 AR3  
M B DQ51 AN2  
M B DQ52 AY2  
M B DQ53 AV1  
M B DQ54 AP3  
M B DQ55 AR1  
M B DQ56 AL1  
M B DQ57 AL2  
M B DQ58 AJ1  
M B DQ59 AH1  
M B DQ60 AM2  
M B DQ61 AM3  
M B DQ62 AH3  
M B DQ63 AJ3

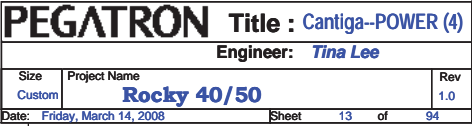
DDR SYSTEM MEMORY B

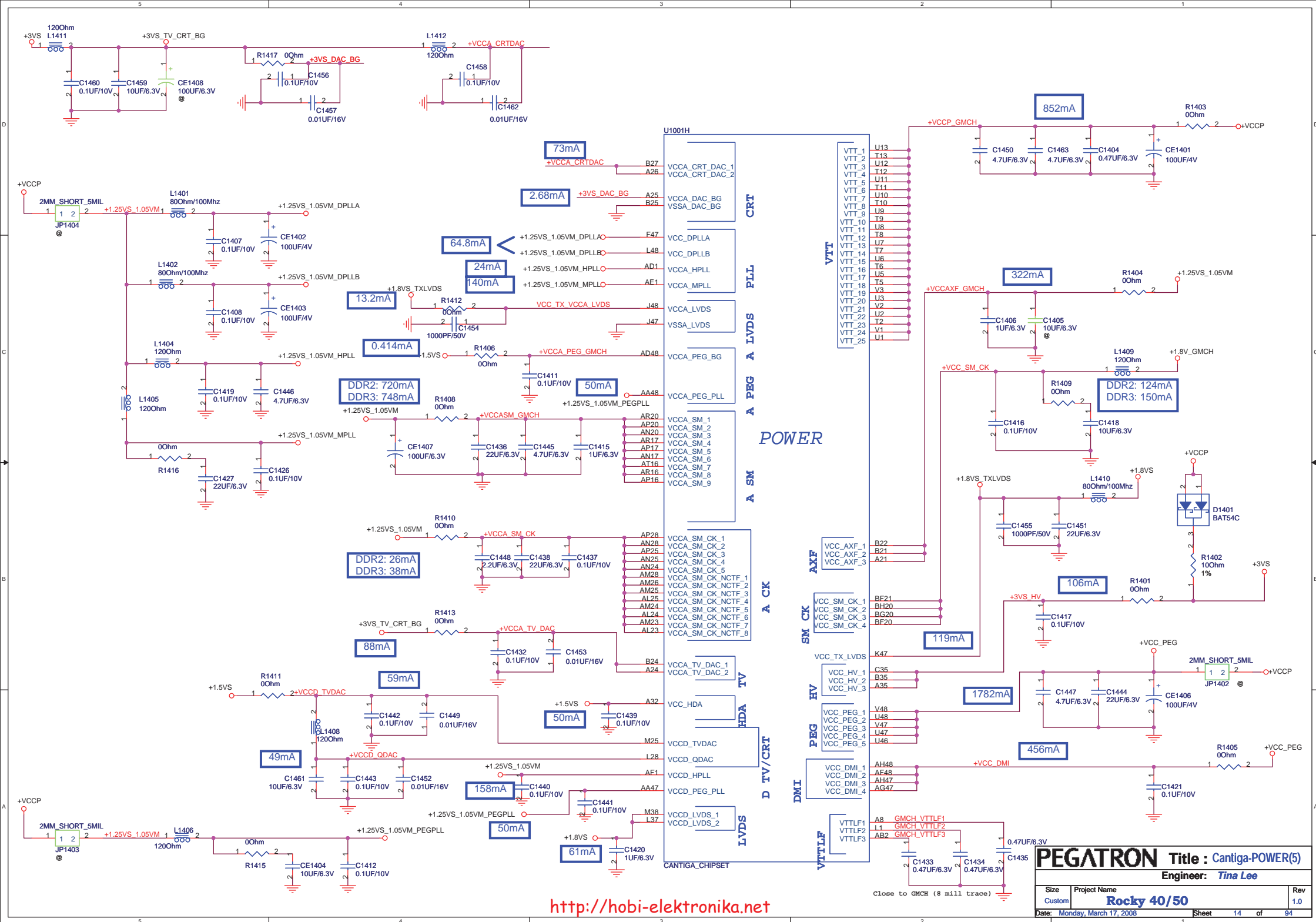
SB\_BS\_0  
SB\_BS\_1  
SB\_BS\_2  
SB\_RAS#  
SB\_CAS#  
SB\_WE#  
SB\_DM\_0  
SB\_DM\_1  
SB\_DM\_2  
SB\_DM\_3  
SB\_DM\_4  
SB\_DM\_5  
SB\_DM\_6  
SB\_DM\_7  
SB\_DQS\_0  
SB\_DQS\_1  
SB\_DQS\_2  
SB\_DQS\_3  
SB\_DQS\_4  
SB\_DQS\_5  
SB\_DQS\_6  
SB\_DQS\_7  
SB\_MA\_0  
SB\_MA\_1  
SB\_MA\_2  
SB\_MA\_3  
SB\_MA\_4  
SB\_MA\_5  
SB\_MA\_6  
SB\_MA\_7  
SB\_MA\_8  
SB\_MA\_9  
SB\_MA\_10  
SB\_MA\_11  
SB\_MA\_12  
SB\_MA\_13  
SB\_MA\_14

BC16 M\_B\_BS0 8,9  
BB17 M\_B\_BS1 8,9  
BB33 M\_B\_BS2 8,9  
AU17 M\_B\_RAS# 8,9  
BG16 M\_B\_CAS# 8,9  
BF14 M\_B\_WE# 8,9  
AM47 M\_B\_DM0  
AY47 M\_B\_DM1  
BD40 M\_B\_DM2  
BF35 M\_B\_DM3  
BG11 M\_B\_DM4  
BA3 M\_B\_DM5  
AP1 M\_B\_DM6  
AK2 M\_B\_DM7  
AL47 M\_B\_DQS0  
AV48 M\_B\_DQS1  
BG41 M\_B\_DQS2  
BG37 M\_B\_DQS3  
BH9 M\_B\_DQS4  
BB2 M\_B\_DQS5  
AU1 M\_B\_DQS6  
AN6 M\_B\_DQS7  
AU47 M\_B\_DQS#0  
BH41 M\_B\_DQS#1  
BH37 M\_B\_DQS#2  
BG9 M\_B\_DQS#3  
BG9 M\_B\_DQS#4  
BC2 M\_B\_DQS#5  
AT2 M\_B\_DQS#6  
AN5 M\_B\_DQS#7  
AV17 M\_B\_A0  
BA25 M\_B\_A1  
BC25 M\_B\_A2  
AU25 M\_B\_A3  
AW25 M\_B\_A4  
BB28 M\_B\_A5  
AU28 M\_B\_A6  
AW28 M\_B\_A7  
AT33 M\_B\_A8  
BD33 M\_B\_A9  
BB16 M\_B\_A10  
AV33 M\_B\_A11  
AY33 M\_B\_A12  
BH15 M\_B\_A13  
AU33 M\_B\_A14

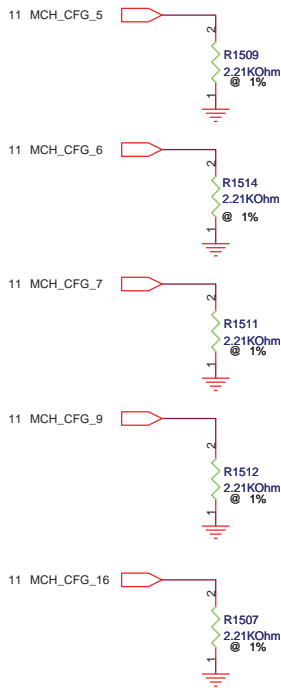
CANTIGA\_CHIPSET

CANTIGA\_CHIPSET









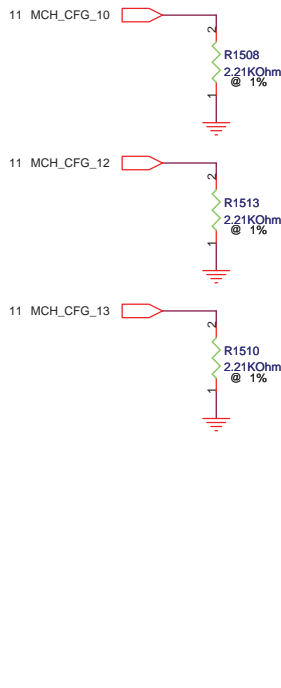
**CFG5 : DMI STRAP**  
**HIGH = DMI X 4 (Default)**  
**LOW = DMI X 2**

**CFG6 : Integrated TPM Host Interface**  
**HIGH = iTPM disable (Default)**  
**LOW = iTPM enable**

**CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite**  
**HIGH = With confidentiality (Default)**  
**LOW = Without confidentiality**

**CFG9 : PCIE GRAPHIC LANE**  
**LOW = Reverse Lanes**  
**HIGH = Normal Operation (Default)**

**CFG16 : FSB Dynamic ODT**  
**HIGH = Enable (Default)**  
**LOW = Disable**

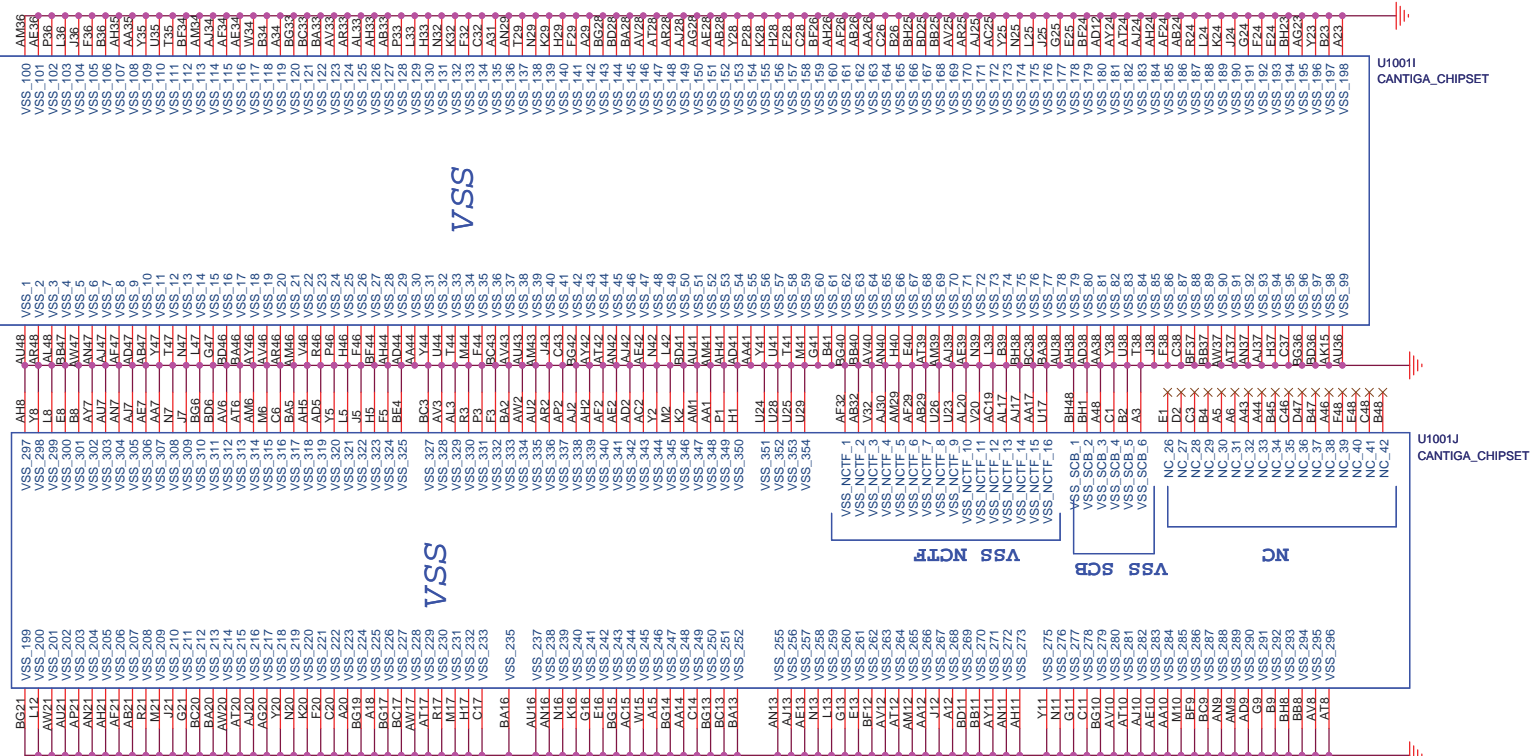


**CFG10 : PCIe Loopback**  
**HIGH = Disable (Default)**  
**LOW = Enable**

**CFG [13:12] : XOR/ALL-Z**  
**00 = Reserved**  
**01 = XOR Mode Enabled**  
**10 = All-Z Mode Enabled**  
**11 = Normal Operation (Default)**

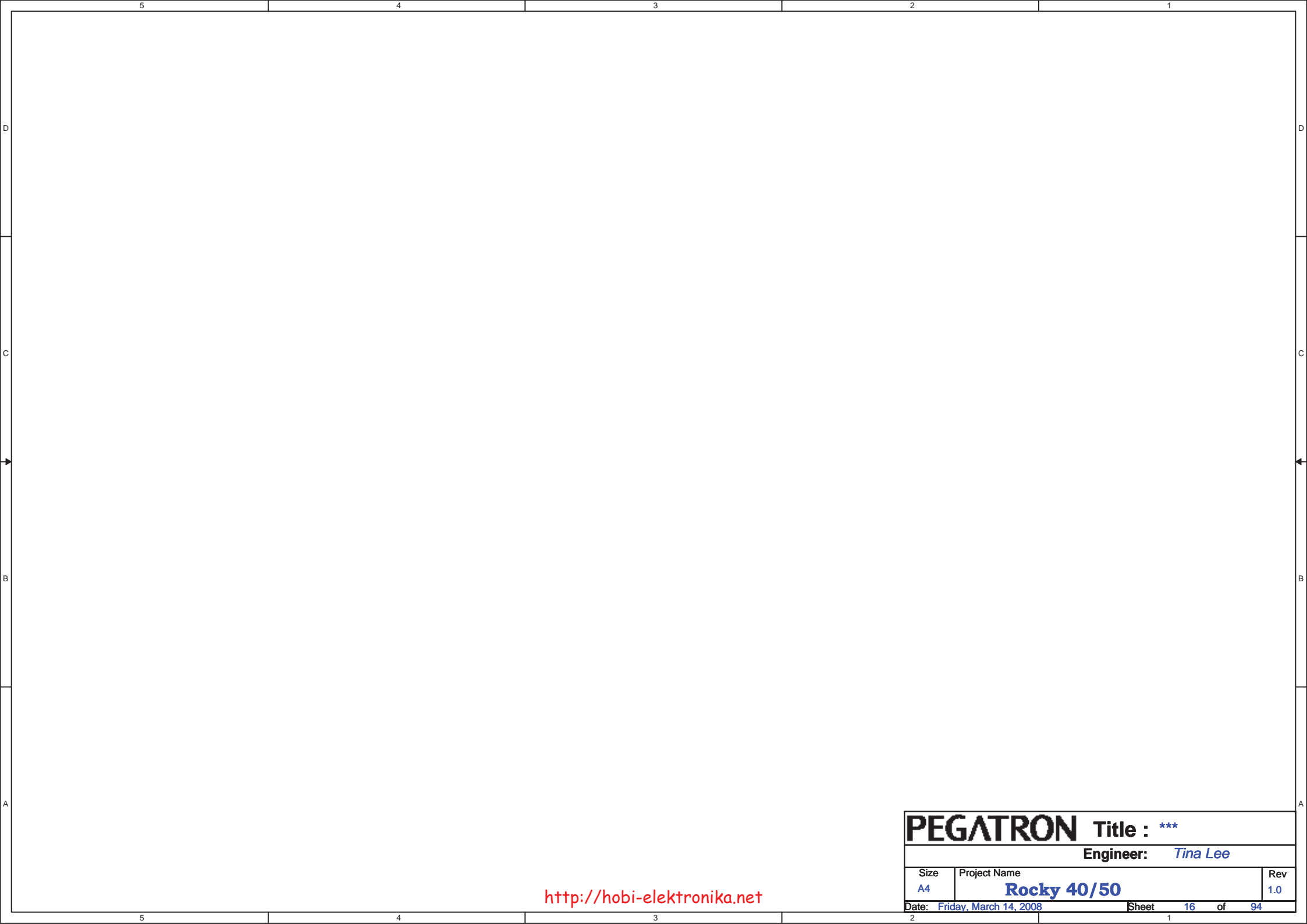
**CFG19 : DMI Lane Reversal**  
**LOW = NORMAL (default)**  
**HIGH = Reverse Lanes**

**CFG20 : SDVO/PCIE CONCURRENT MODE**  
**LOW = ONLY SDVO or PCIE is Operational (Default)**  
**HIGH = SDVO and PCIE are operating simultaneously via the PEG port**



U1001J  
CANTIGA\_CHIPSET

U1001I  
CANTIGA\_CHIPSET



PEGATRON			Title : ***		
			Engineer: Tina Lee		
Size		Project Name			Rev
A4		Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	16	of 94



5	4	3	2	1
D				
C				
B				
A				

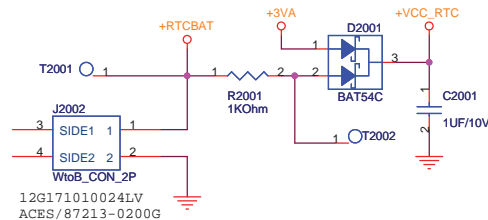
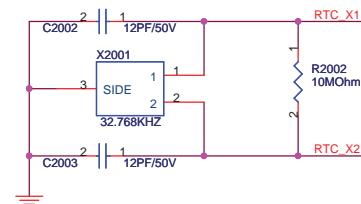
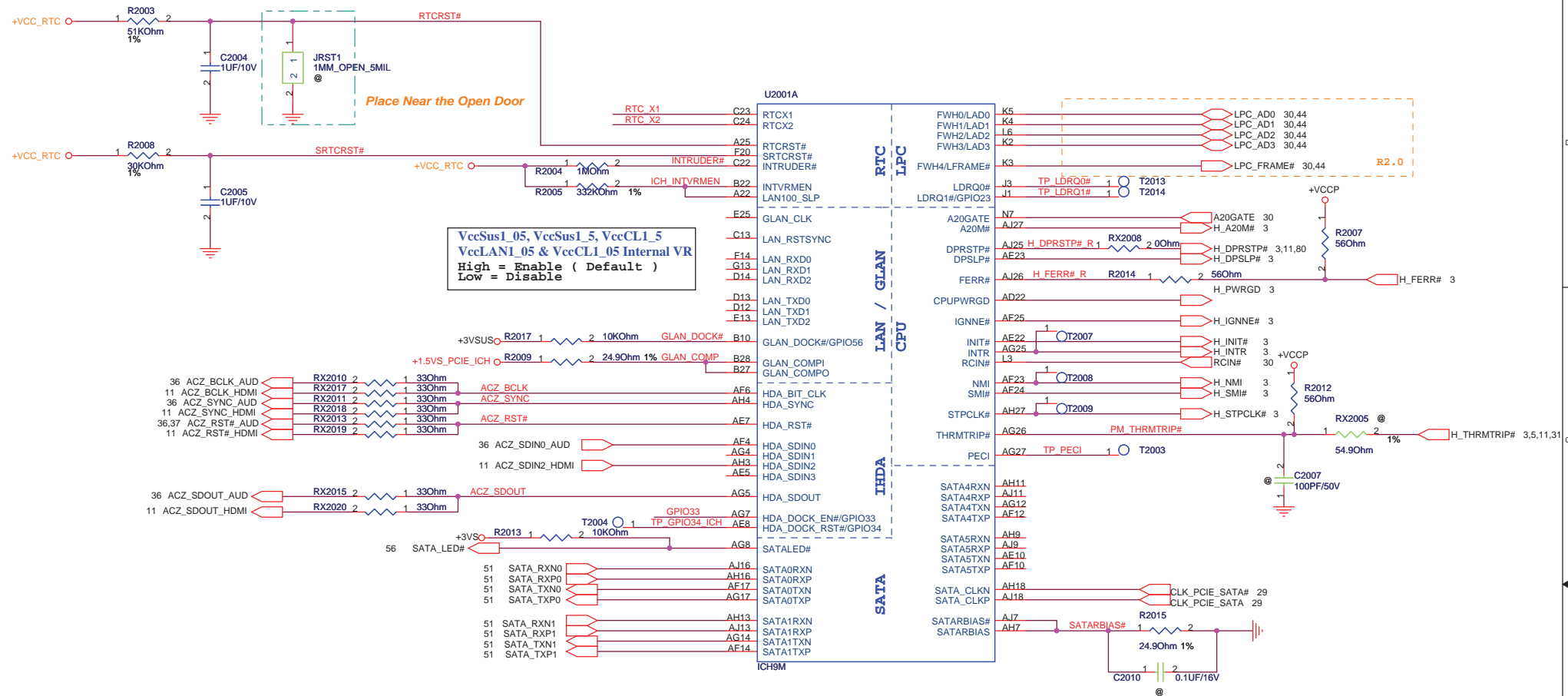
<b>PEGATRON</b>		Title : <b>***</b>	
		Engineer: <b><i>Tina Lee</i></b>	
Size	Project Name		Rev
<b>A4</b>	<b>Rocky 40/50</b>		<b>1.0</b>
Date:	Friday, March 14, 2008		Sheet 17 of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON			Title : ***	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	18 of 94

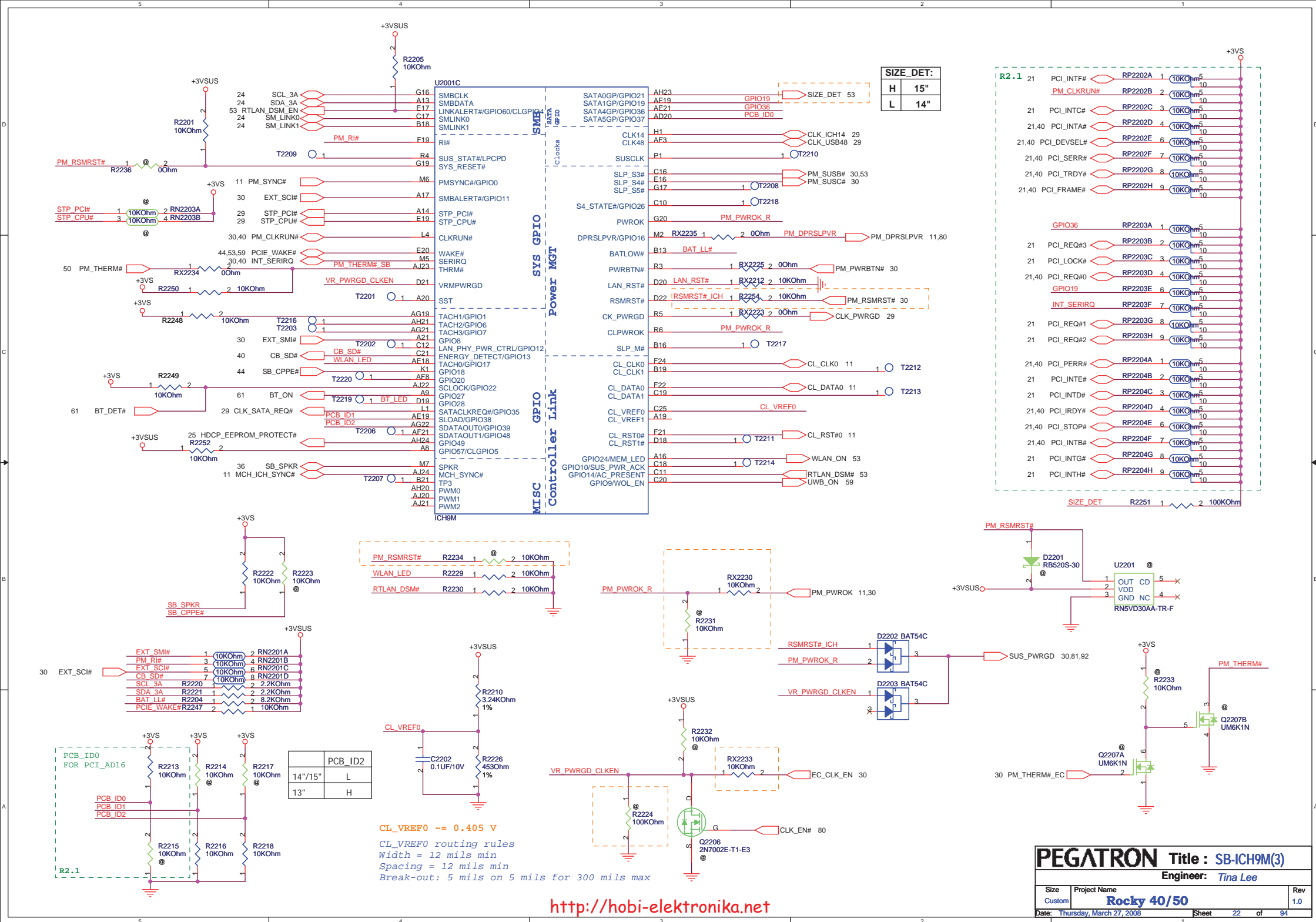
5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON			Title : ***	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	19 of 94



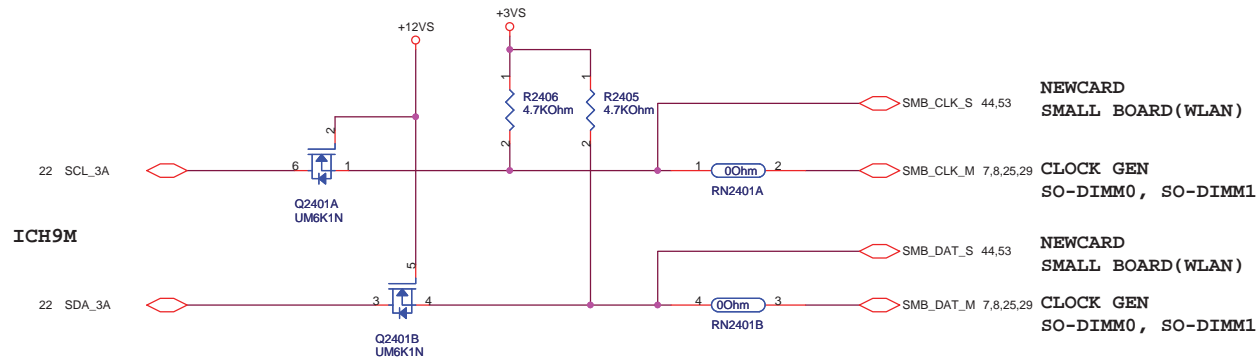
[ICH\_TP3, ACZ\_SDOUT] : XOR Chain Entrance Strap  
 00 = Reserved  
 01 = Enter XOR Chain  
 10 = Normal Operation (Default)  
 11 = Set PCIe Port Config Bit 1



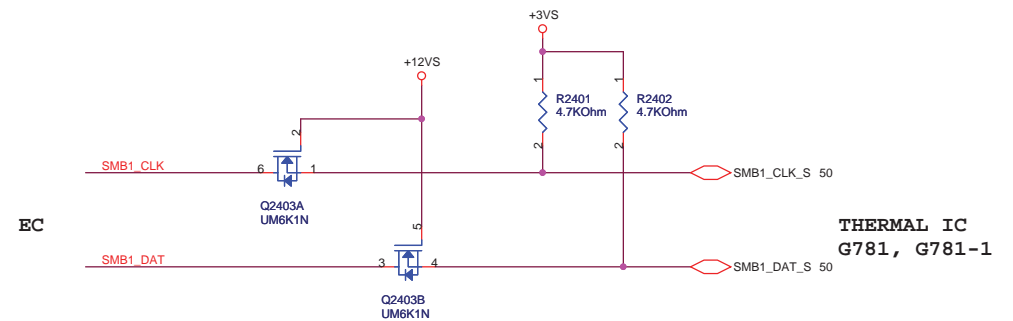
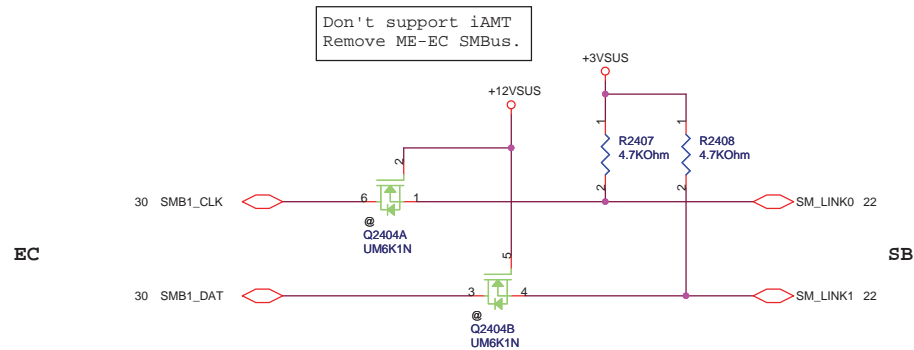




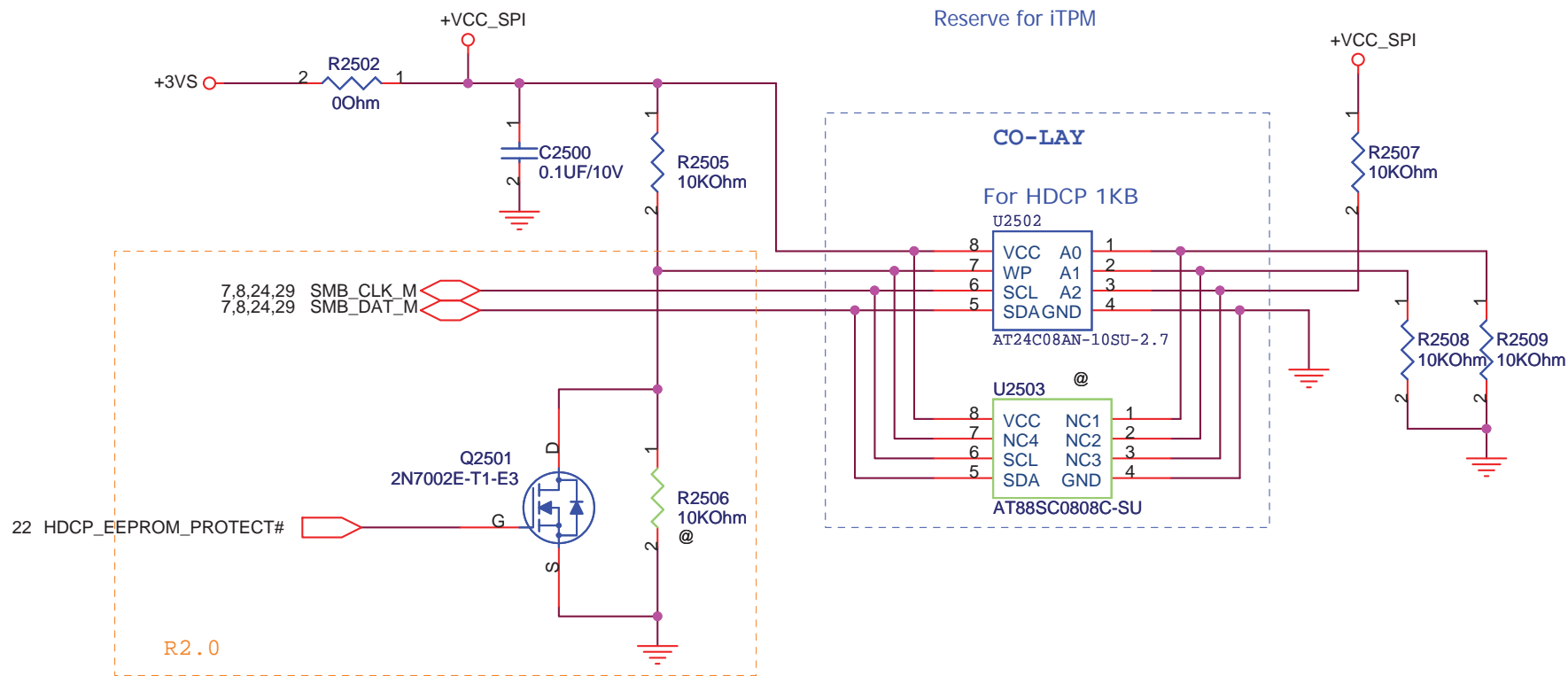
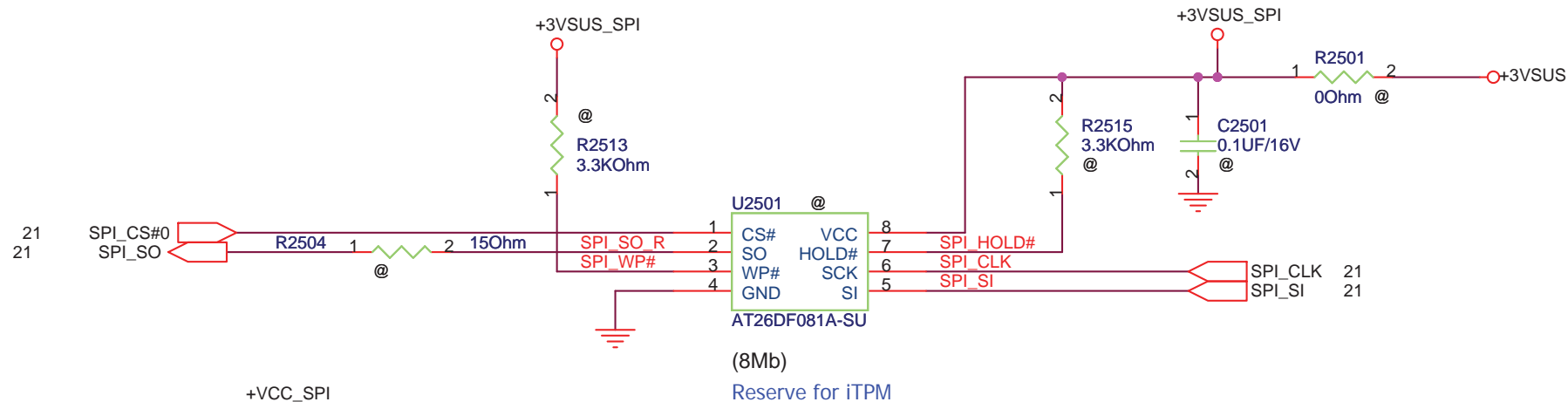
# ICH9-M



# EC



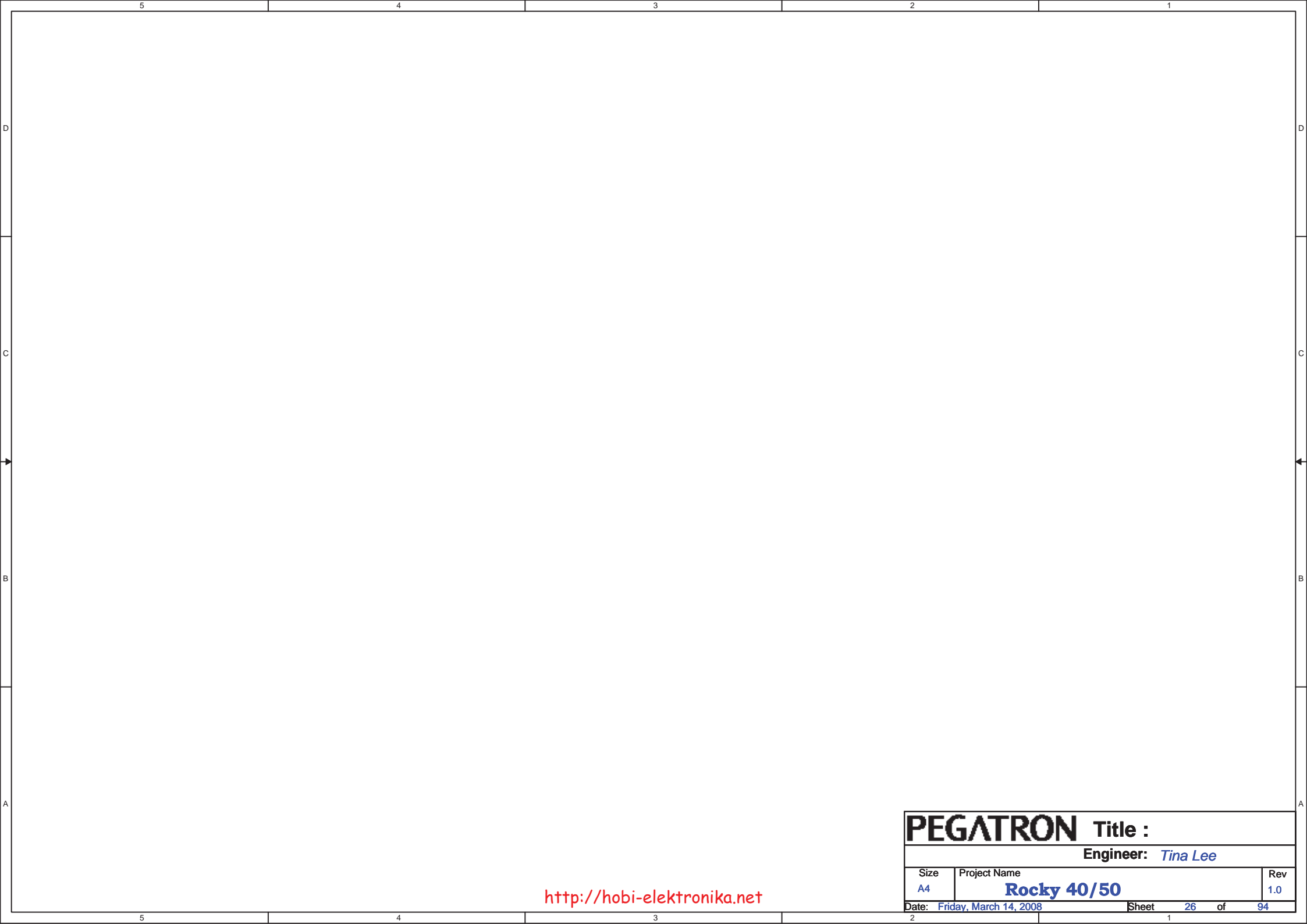




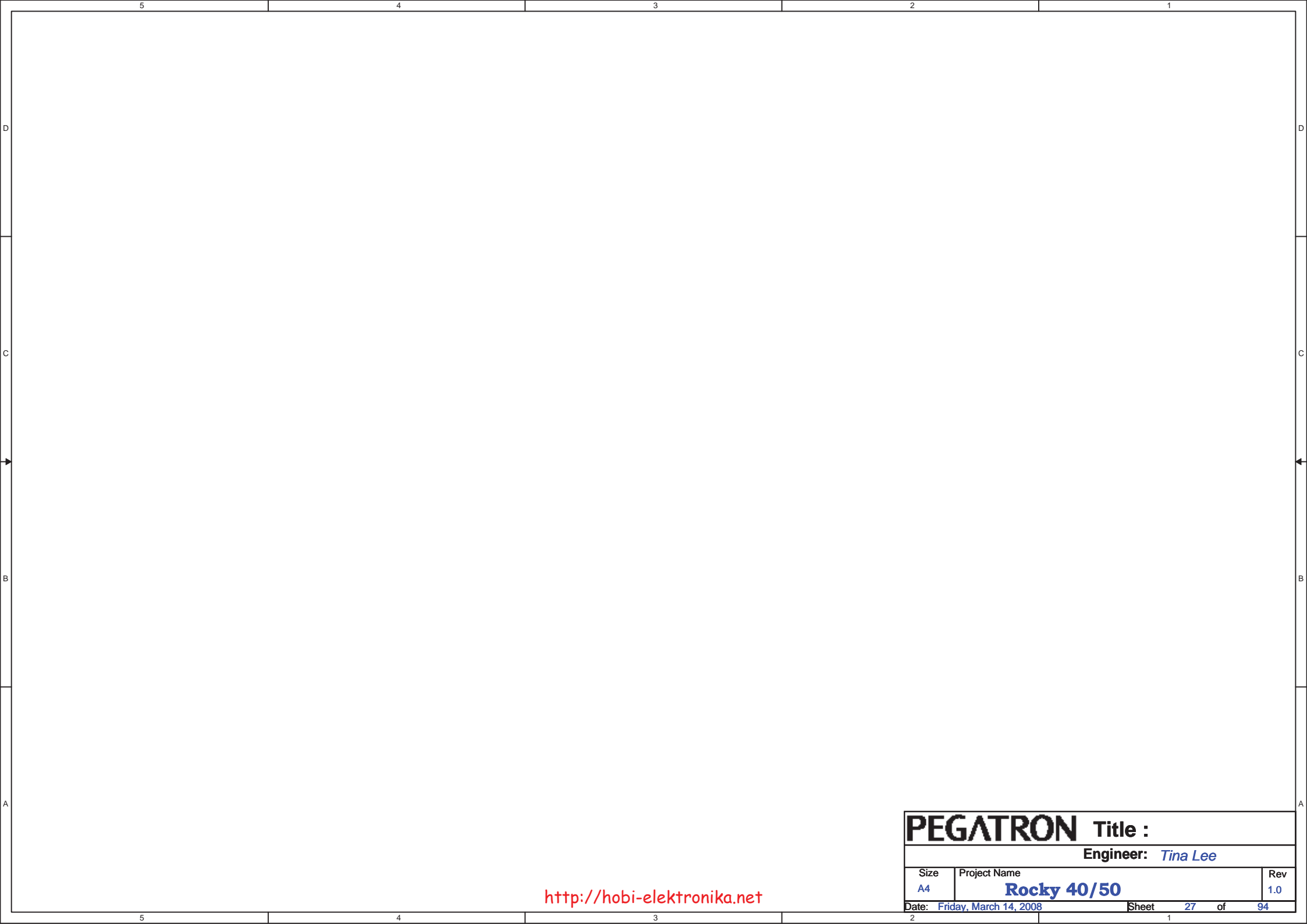
U2502-AT24C08A :  
 Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509  
 Nostuff : R2505

U2503-AT88SC0808C :  
 Stuff : U2503  
 Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

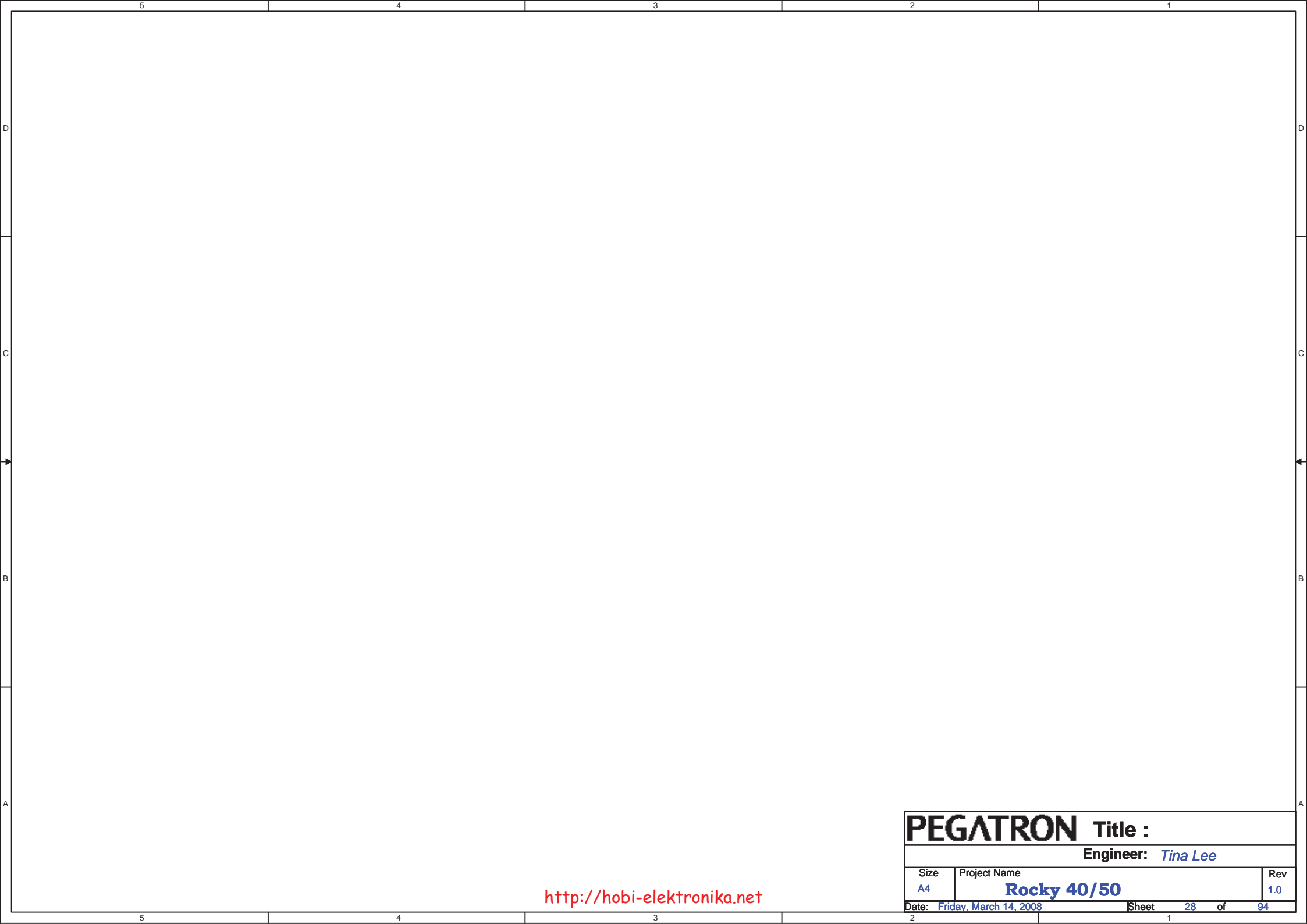
<b>PEGATRON</b>			Title : <b>SPI ROM</b>	
			Engineer: <b>Tina Lee</b>	
Size	Project Name			Rev
Custom	<b>Rocky 40/50</b>			1.0
Date: <b>Thursday, March 27, 2008</b>		Sheet <b>25</b> of <b>94</b>		



PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	26	of 94



<b>PEGATRON</b>			Title :		
			Engineer: <i>Tina Lee</i>		
Size	Project Name				Rev
A4	<b>Rocky 40/50</b>				1.0
Date: <i>Friday, March 14, 2008</i>			Sheet	<i>27</i>	of <i>94</i>



D

D

C

C

B

B

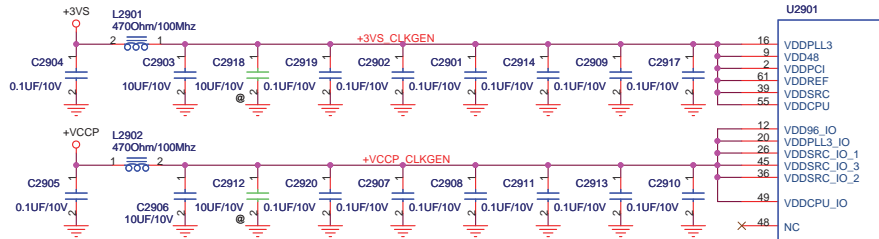
A

A

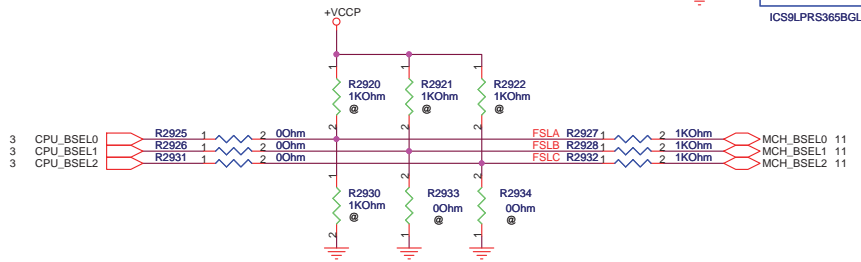
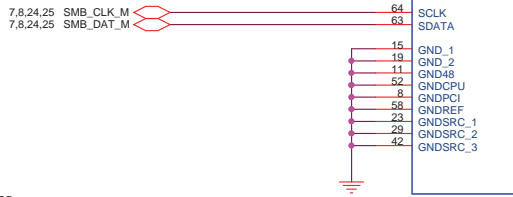
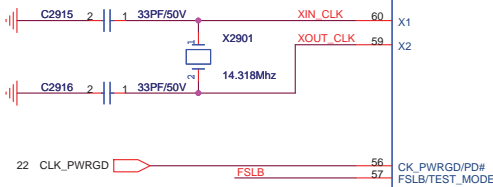
<http://hobi-elektronika.net>

PEGATRON			Title :			
			Engineer: Tina Lee			
Size	Project Name				Rev	
A4	Rocky 40/50				1.0	
Date: Friday, March 14, 2008			Sheet	28	of	94

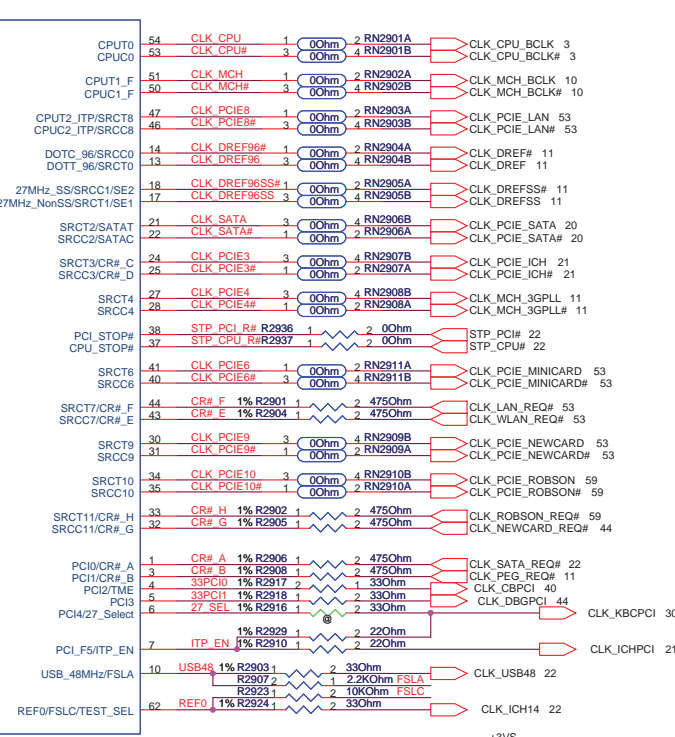
+VCCP ○ +VCCP 5,10,11,13,14,20,23,80,82  
+3VS ○ +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,56,57,58,59,61,91,92



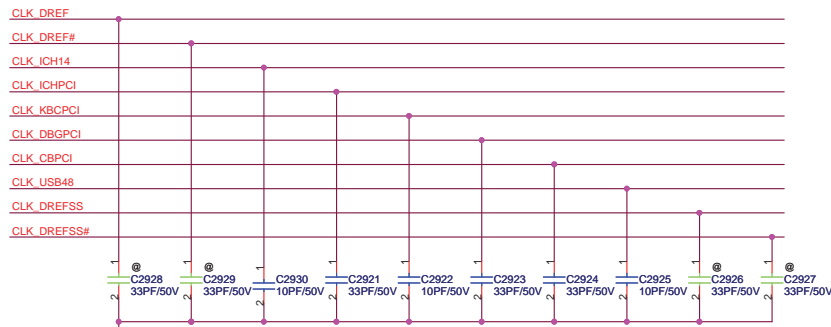
C2917, C2918, C2919 near CLK Gen.



		FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.



<http://hobi-elektronika.net>

CR#_A	0 = SRC 0	
	1 = SRC 2	SATA
CR#_B	0 = SRC 1	
	1 = SRC 4	MCH
CR#_C	0 = SRC 0	
	1 = SRC 2	
CR#_D	0 = SRC 1	
	1 = SRC 4	
CR#_E	SRC 6	WLAN
CR#_F	SRC 8	LAN
CR#_G	SRC 9	New Card
CR#_H	SRC 10	Robson

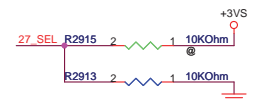
## Latched Input Select

0 = SRC 8 Decide pin  
1 = CPU\_ITP CLK 46, 47



27\_Select=0, Decide pin  
pin#13/14=DOT96; 13/14, 17/18  
pin#17/18=LCD\_SST;

27\_Select=1, Decide pin  
pin#13/14=SRC0; 13/14, 17/18  
pin#17/18=27MHz non-spread SE clock;

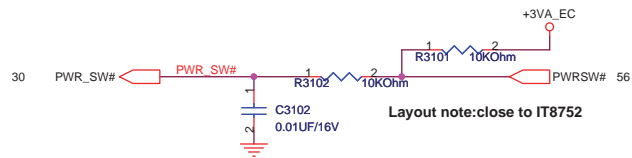


For GM/GL, need to PD for 96MHz output.  
For PM, need to PU for 27MHz output.

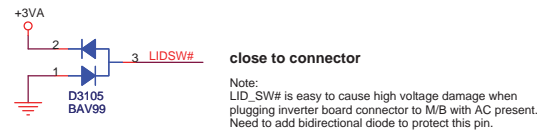
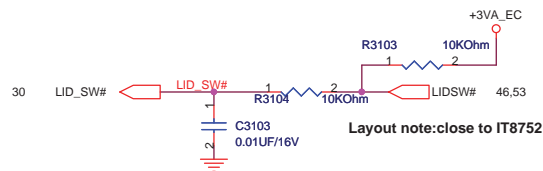


## For Switch

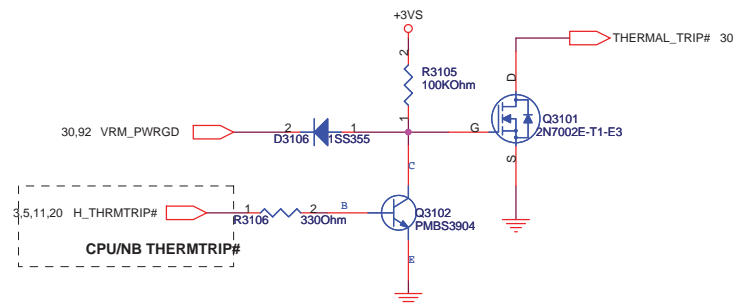
### PWR SWITCH



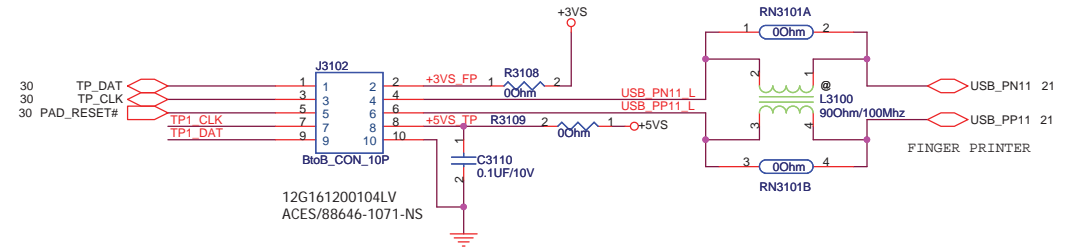
### LID SWITCH



## For Thermal Control Method

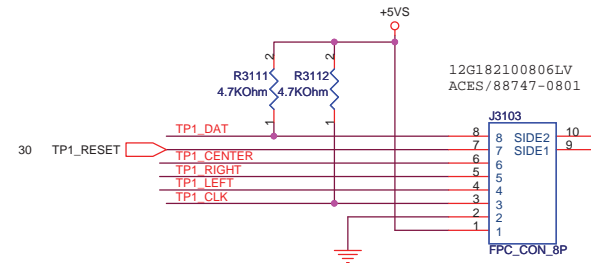


## TOUCH PAD CONN

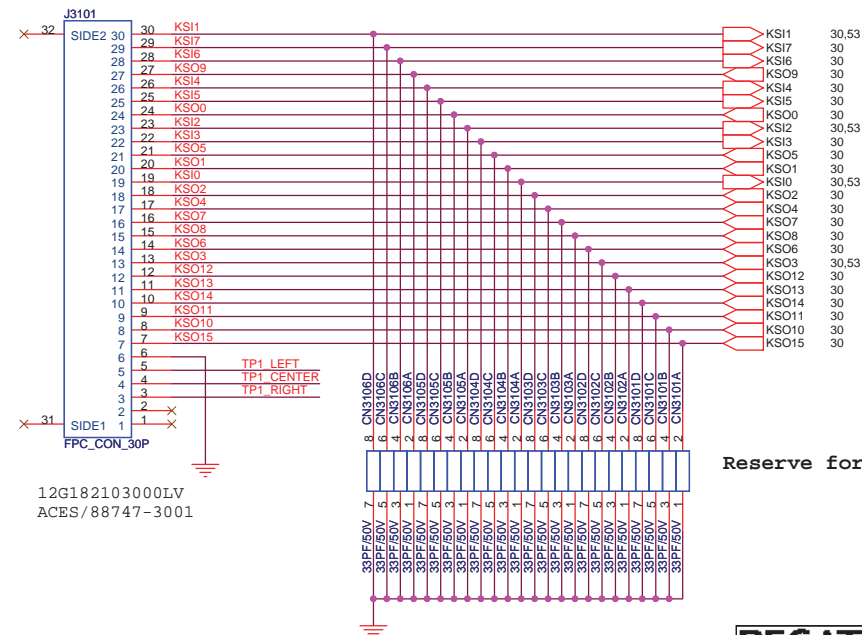


TP :Touch Pad  
TP1:Trach Point

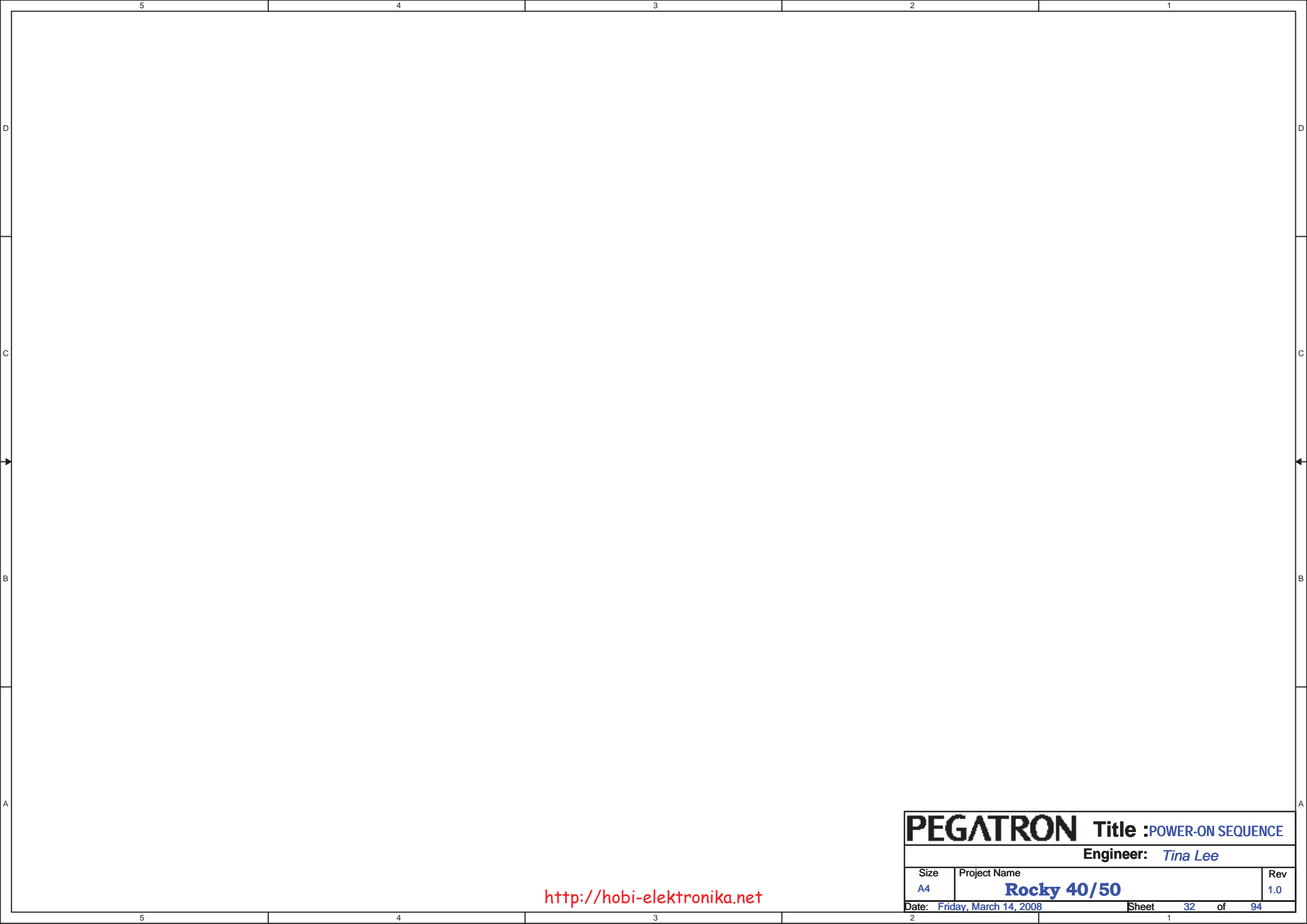
## TRACK POINT CONN



## Keyboard Connector



Reserve for WWAN



D

C

B

A

D

C

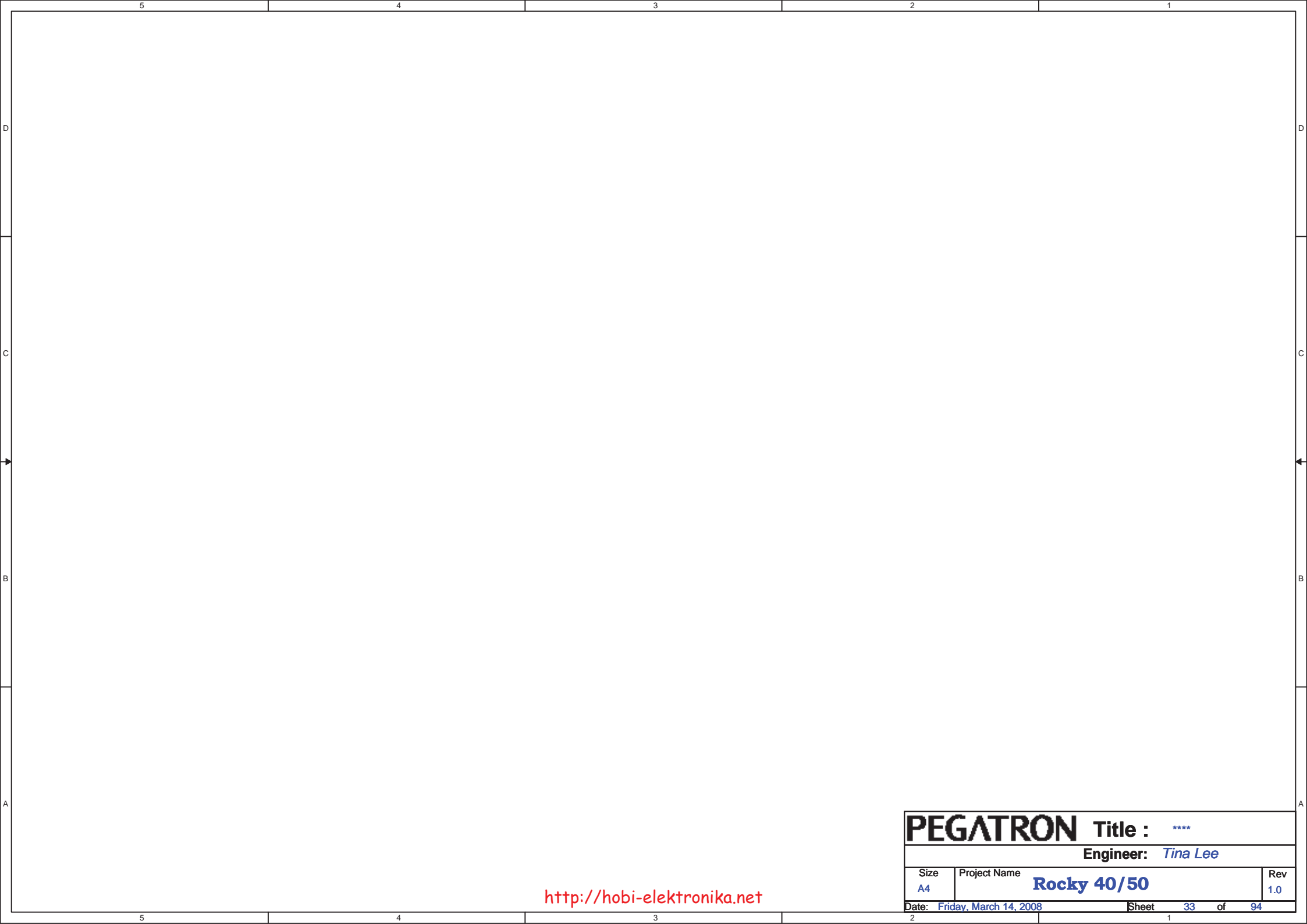
B

A



<b>PEGATRON</b>		<b>Title :</b> POWER-ON SEQUENCE	
<b>Engineer:</b> Tina Lee			
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008		Sheet 32	of 94

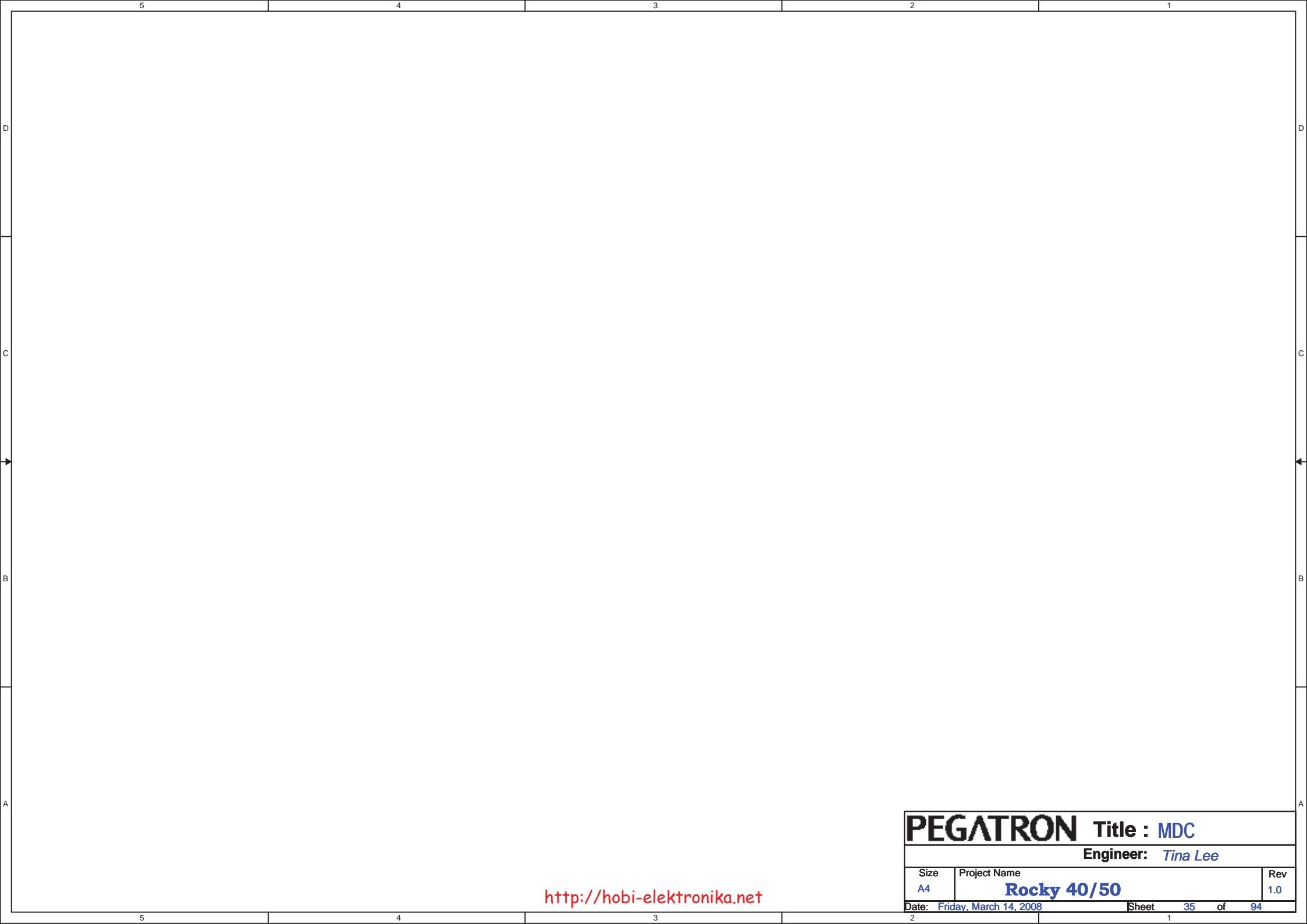




<b>PEGATRON</b>		Title : ****	
Engineer: Tina Lee			
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008	Sheet	33	of 94

5	4	3	2	1
D				
C				
B				
A				

<b>PEGATRON</b>		Title : ****	
<Variant Name>		Engineer: Tina Lee	
Size A4	Project Name Rocky 40/50		Rev 1.0
Date: Friday, March 14, 2008		Sheet	34 of 94



D

C

B

A

D

C

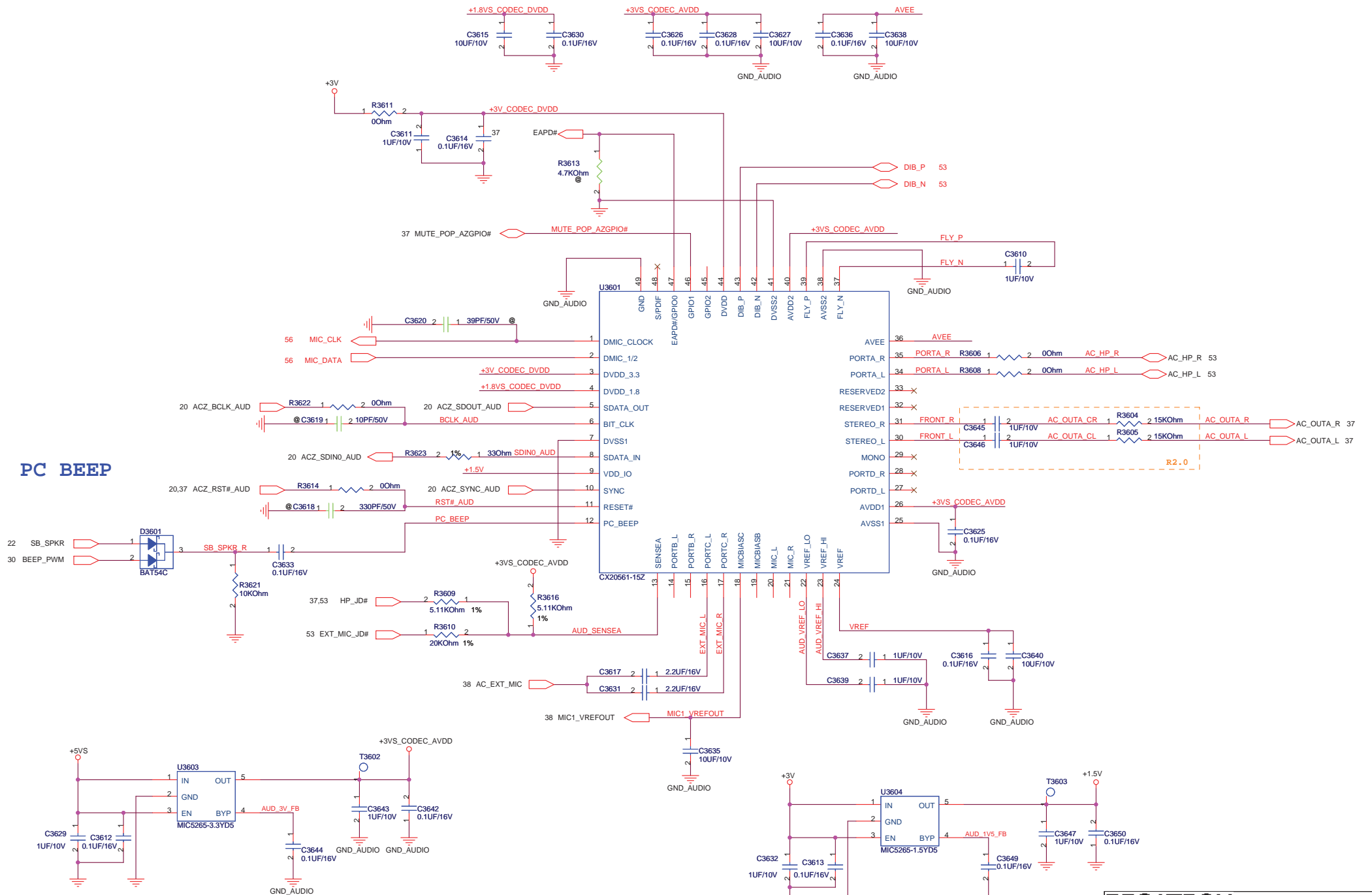
B

A



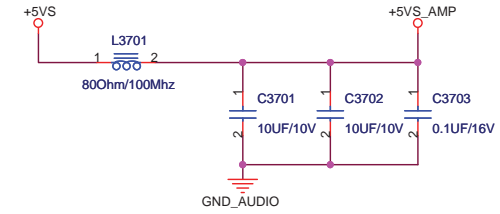
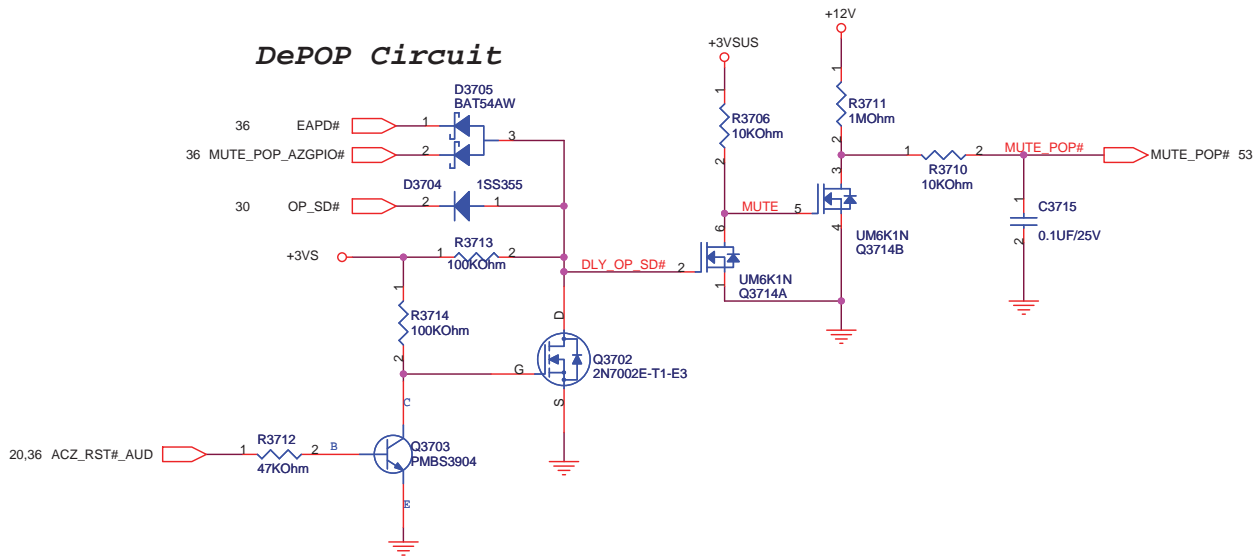
<http://hobi-elektronika.net>

<b>PEGATRON</b>		Title : <b>MDC</b>	
		Engineer: <i>Tina Lee</i>	
Size <i>A4</i>	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: <i>Friday, March 14, 2008</i>		Sheet	<i>35</i> of <i>94</i>

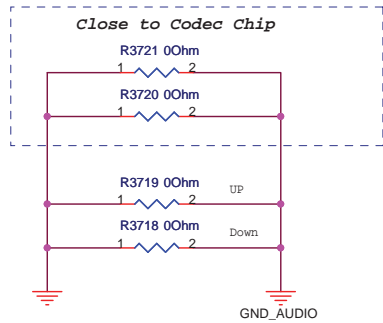


PEGATRON				Title : CODEC CX20561	
				Engineer: Tina Lee	
Size	Project Name				Rev
Custom		Rocky 40/50			1.0
Date: Thursday, March 27, 2008		Sheet		36	of 94

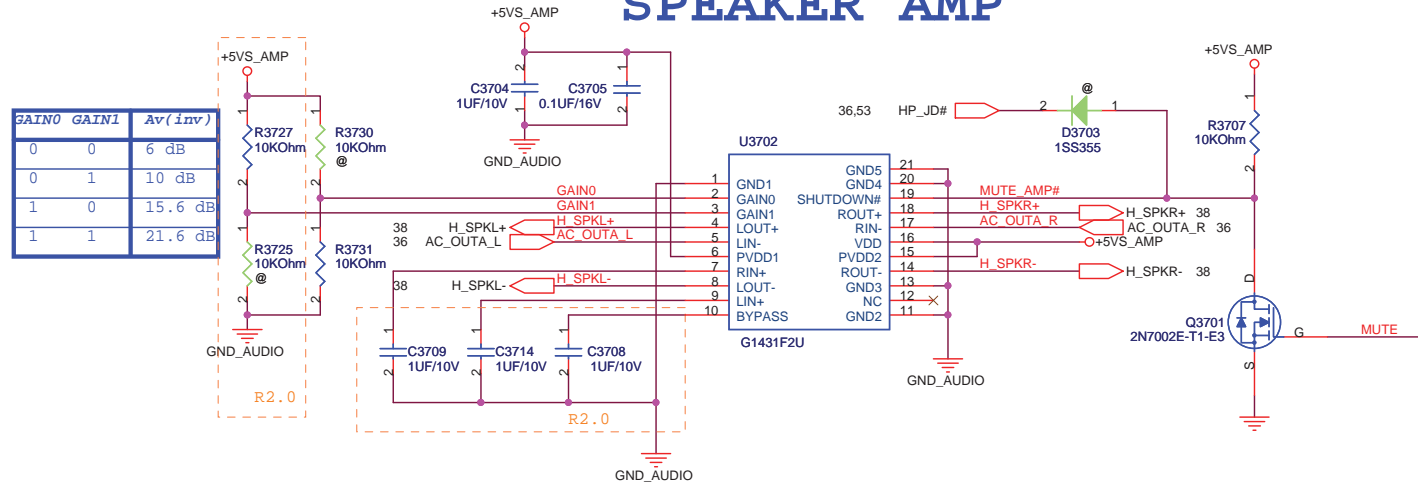
## DePOP Circuit



## JACK GND



## SPEAKER AMP



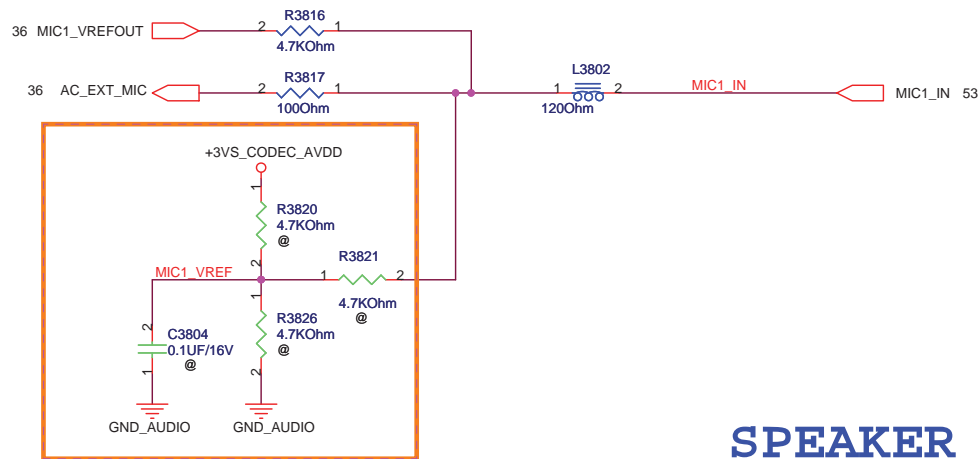
GAIN0	GAIN1	Av( inv )
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

**PEGATRON** Title : **AUDIO AMP**

Engineer: **Tina Lee**

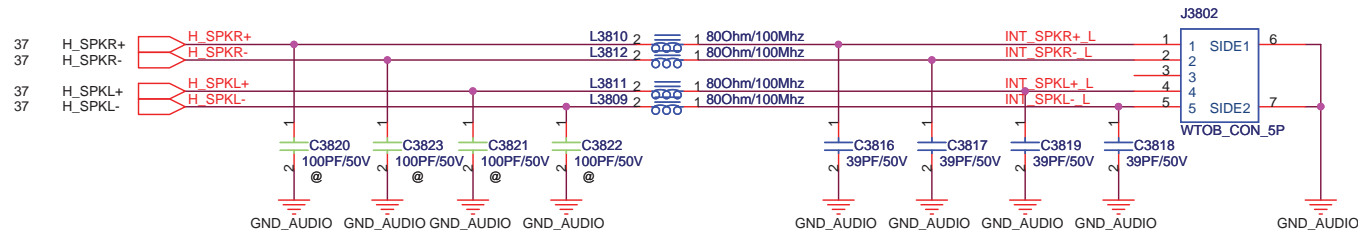
Size Custom	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Thursday, March 27, 2008	Sheet 37	of 94

# EXT MICROPHONE

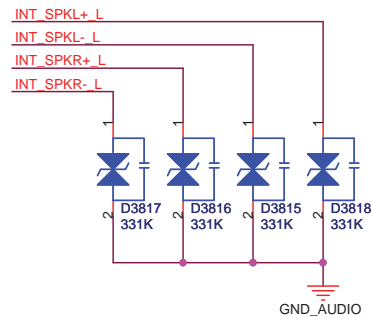


Reserved the external MIC bias(T filter).

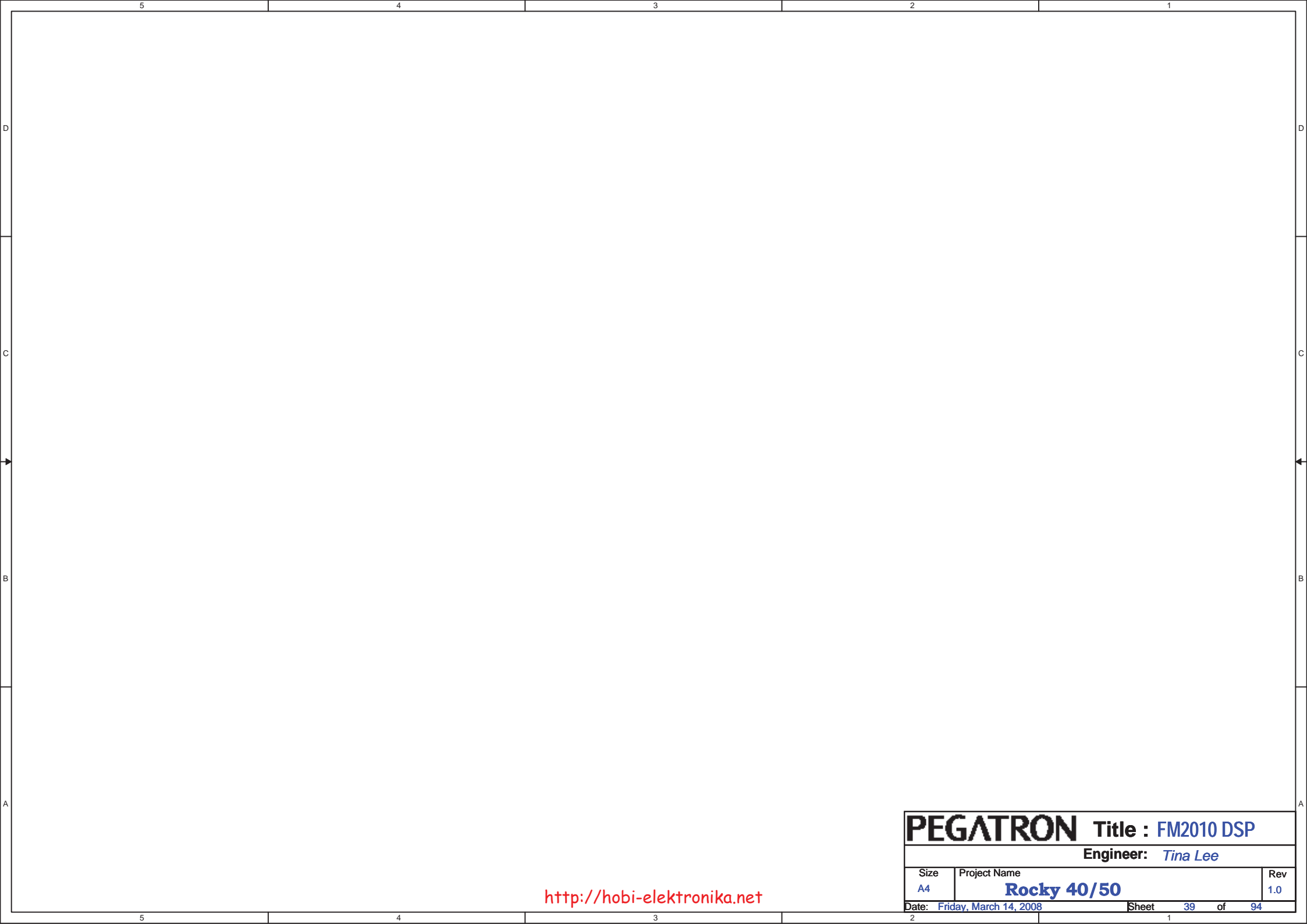
# SPEAKER CONNECTOR



12G171010050LV  
ACES/87213-0500G



<b>PEGATRON</b>		Title : <b>MIC&amp;LINEIN</b>	
		Engineer: <b>Tina Lee</b>	
Size Custom	Project Name <b>Rocky 40/50</b>	Rev 1.0	
Date: Thursday, March 27, 2008		Sheet	38 of 94



D

C

B

A

D

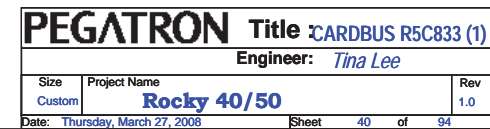
C

B

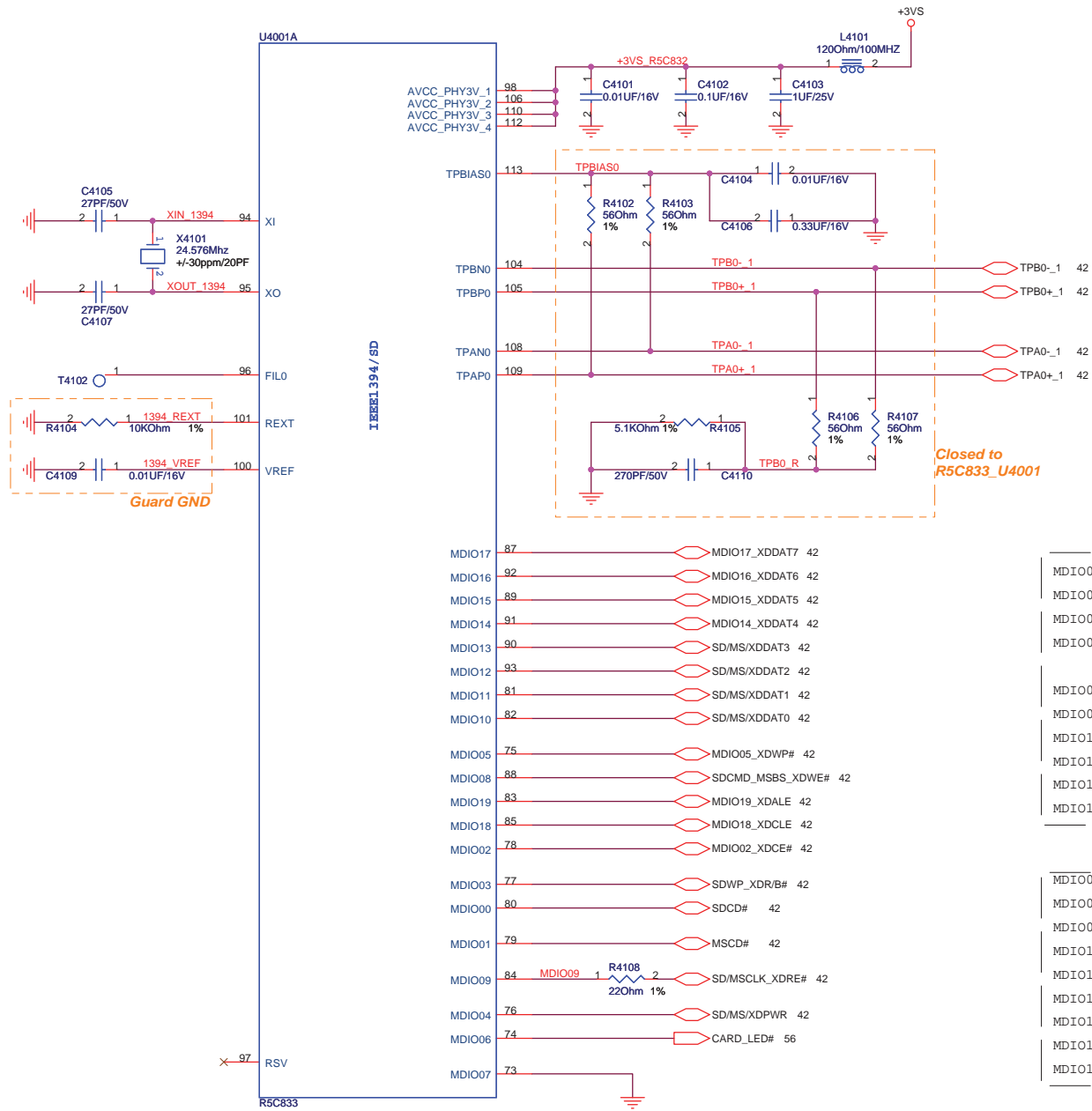
A

<http://hobi-elektronika.net>

<b>PEGATRON</b>		<b>Title :</b> FM2010 DSP	
		<b>Engineer:</b> Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	39 of 94

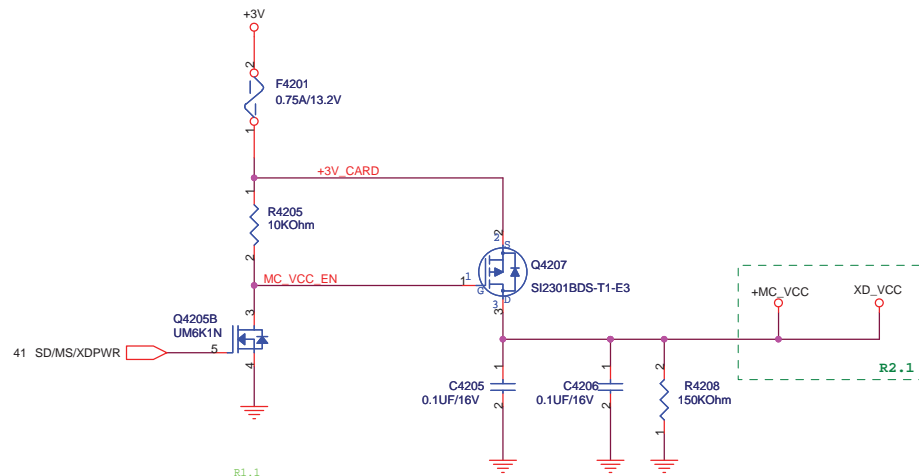




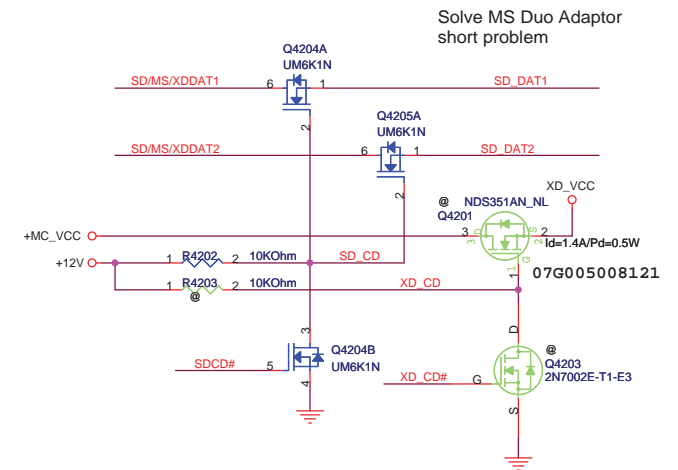
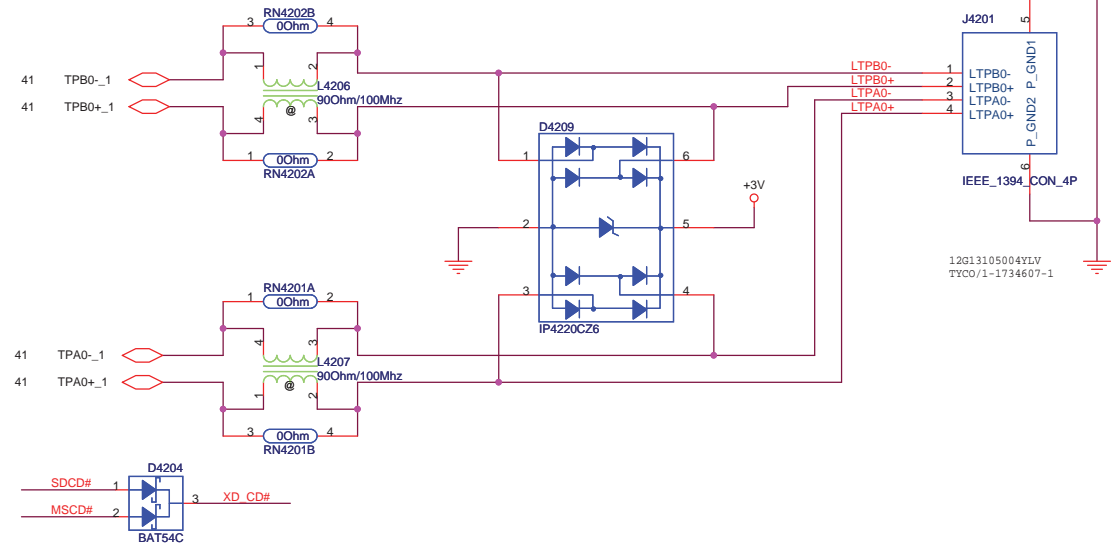
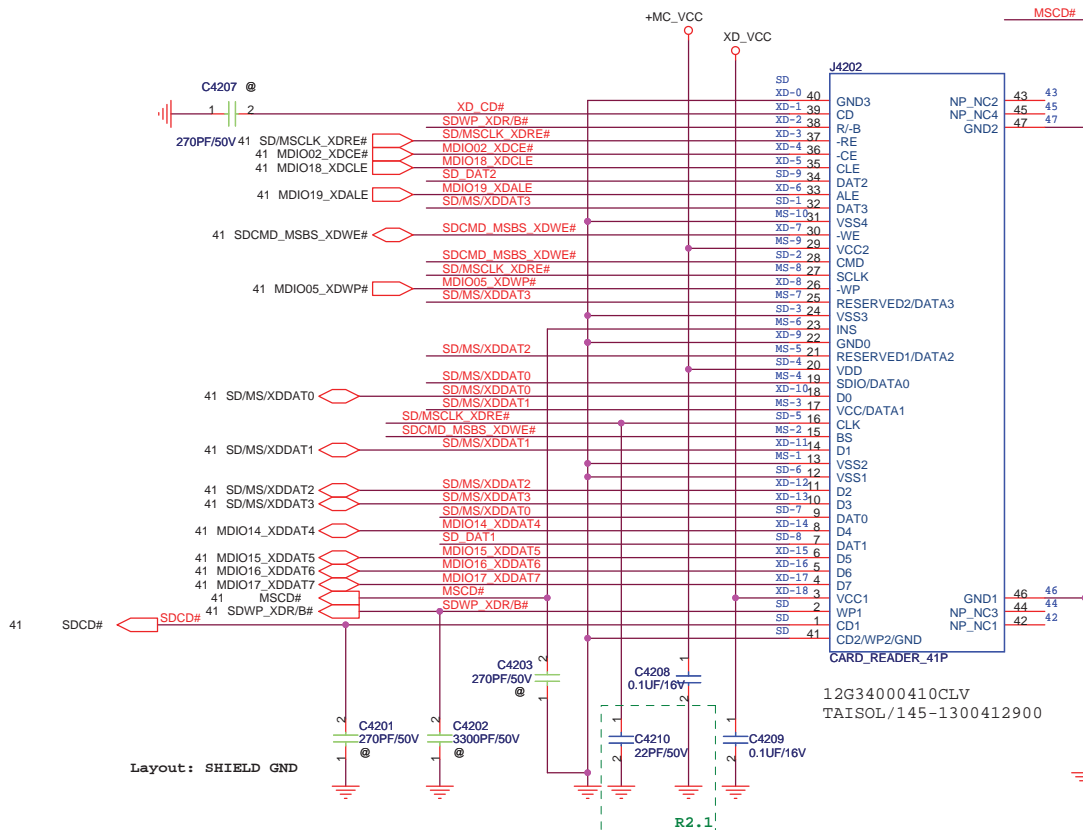


MDIO00--> SD Card Detect  
MDIO01--> MS Card Detect  
MDIO03--> SD Write Protect  
MDIO04--> SD Card Power0 Control/  
MS Power Control  
MDIO08--> SD Command/MS Bus State  
MDIO09--> SD Clock/MS Clock  
MDIO10--> SD Data 0/MS Data 0  
MDIO11--> SD Data 1/MS Data 1  
MDIO12--> SD Data 2/MS Data 2  
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#  
MDIO05--> SD Power Control 1 / xDWP  
MDIO06--> xD/MS/SD LED Control  
MDIO14--> xD Data  
MDIO15--> xD Data  
MDIO16--> xD Data  
MDIO17--> xD Data  
MDIO18--> xD CLE  
MDIO19--> xD ALE



Place as close to  
card reader socket  
as possible





D

D

C

C

B

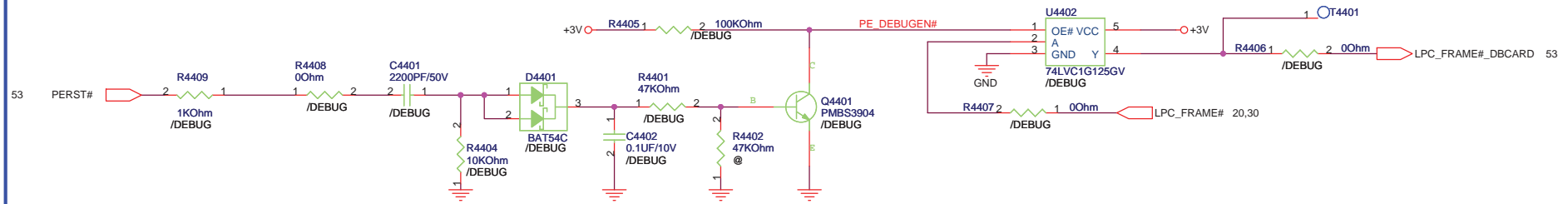
B

A

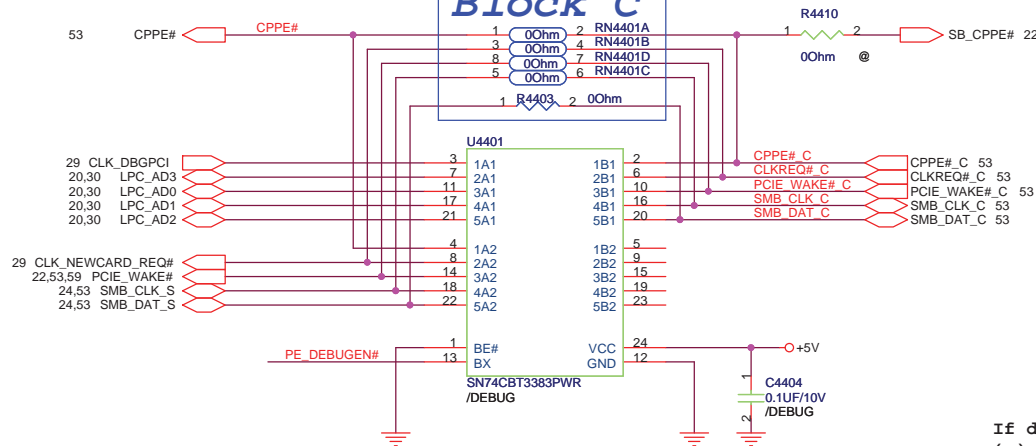
A

<b>PEGATRON</b>		<b>Title :</b> NEW CARD	
		<b>Engineer:</b> Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	43 of 94

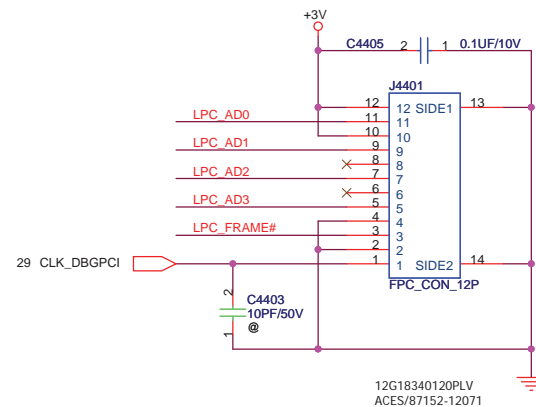
# Block A



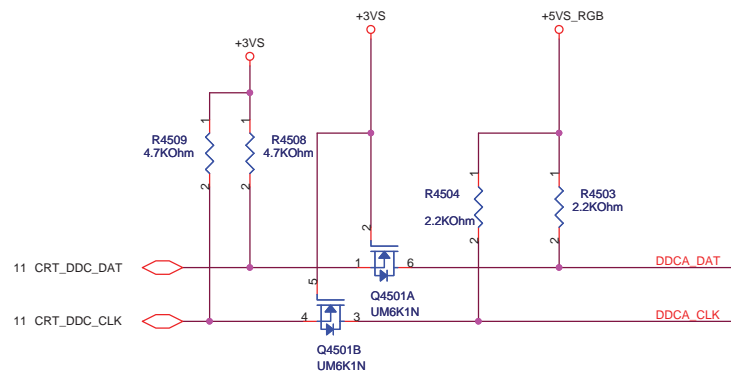
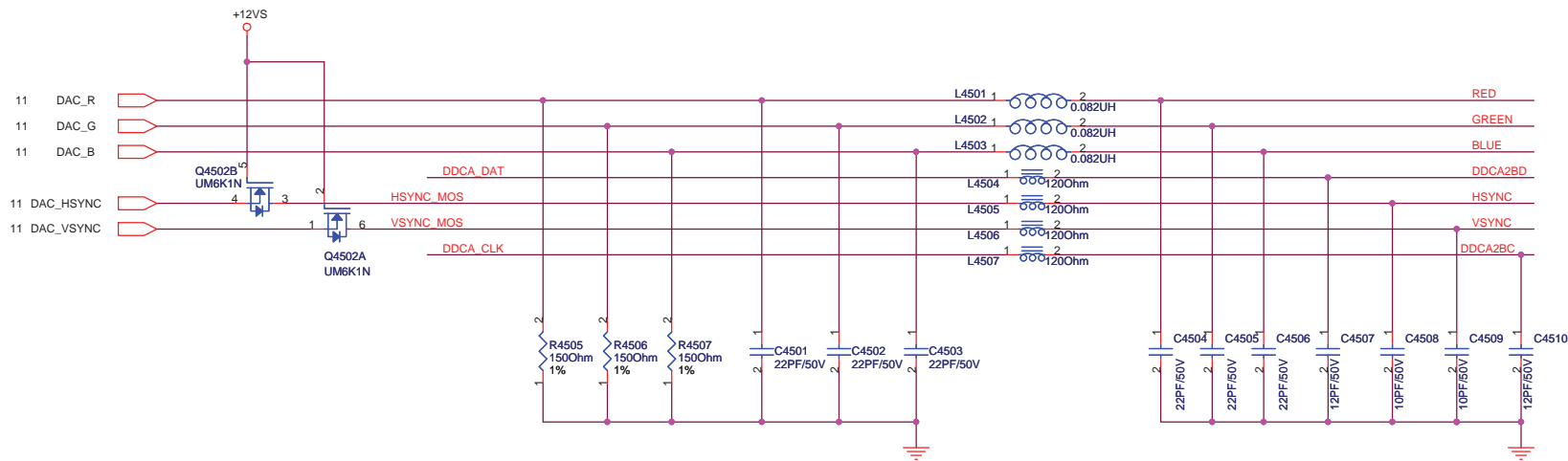
# Block C



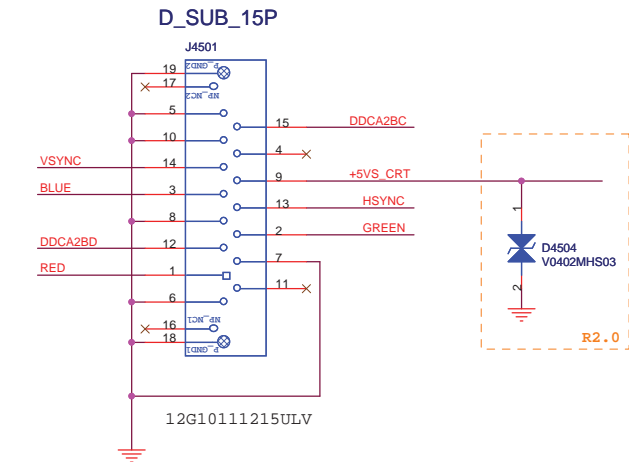
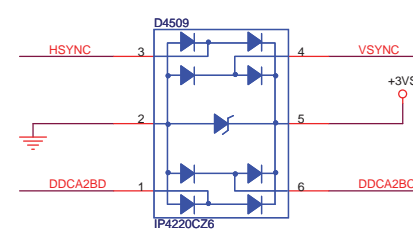
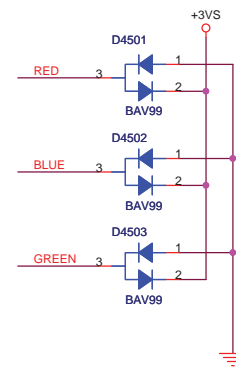
If don't support NewCard Debug Card,Pls do  
(a) DNI all components of block A  
(b) Mount Block C (RN5401,R6975)



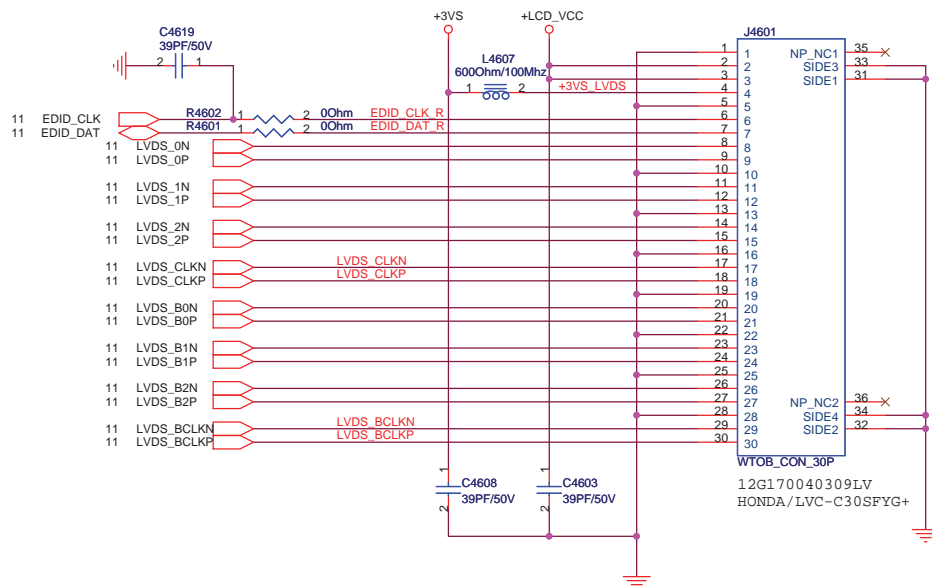
PEGATRON		Title : DEBUG	
Size		Engineer: Tina Lee	
Custom	Project Name	Rocky 40/50	
Date: Thursday, March 27, 2008	Sheet	44	of 94
		Rev	1.0



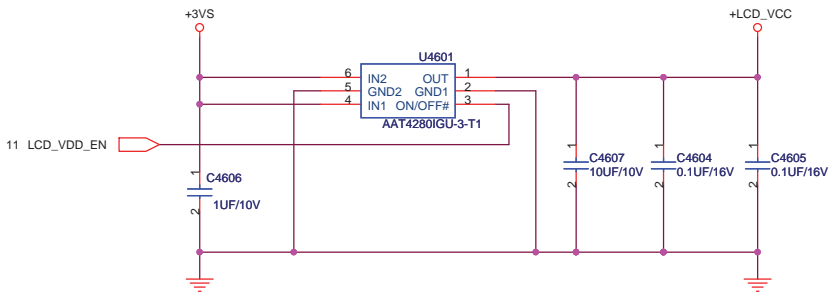
PLACE ESD Diodes near VGA port



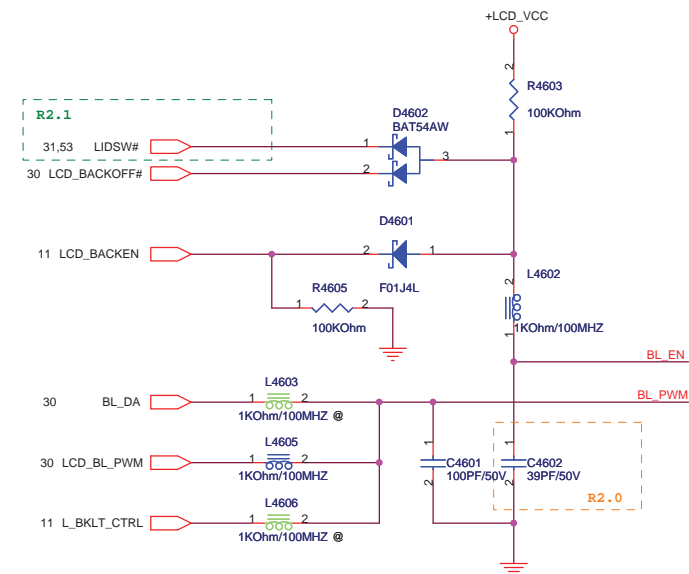
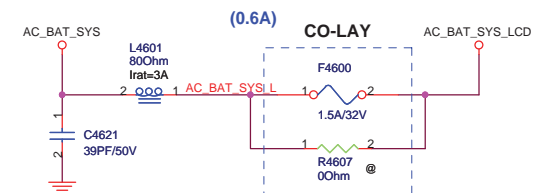
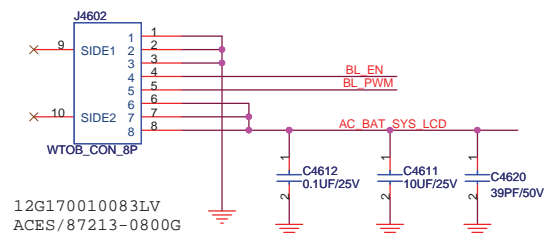
## LVDS CNT

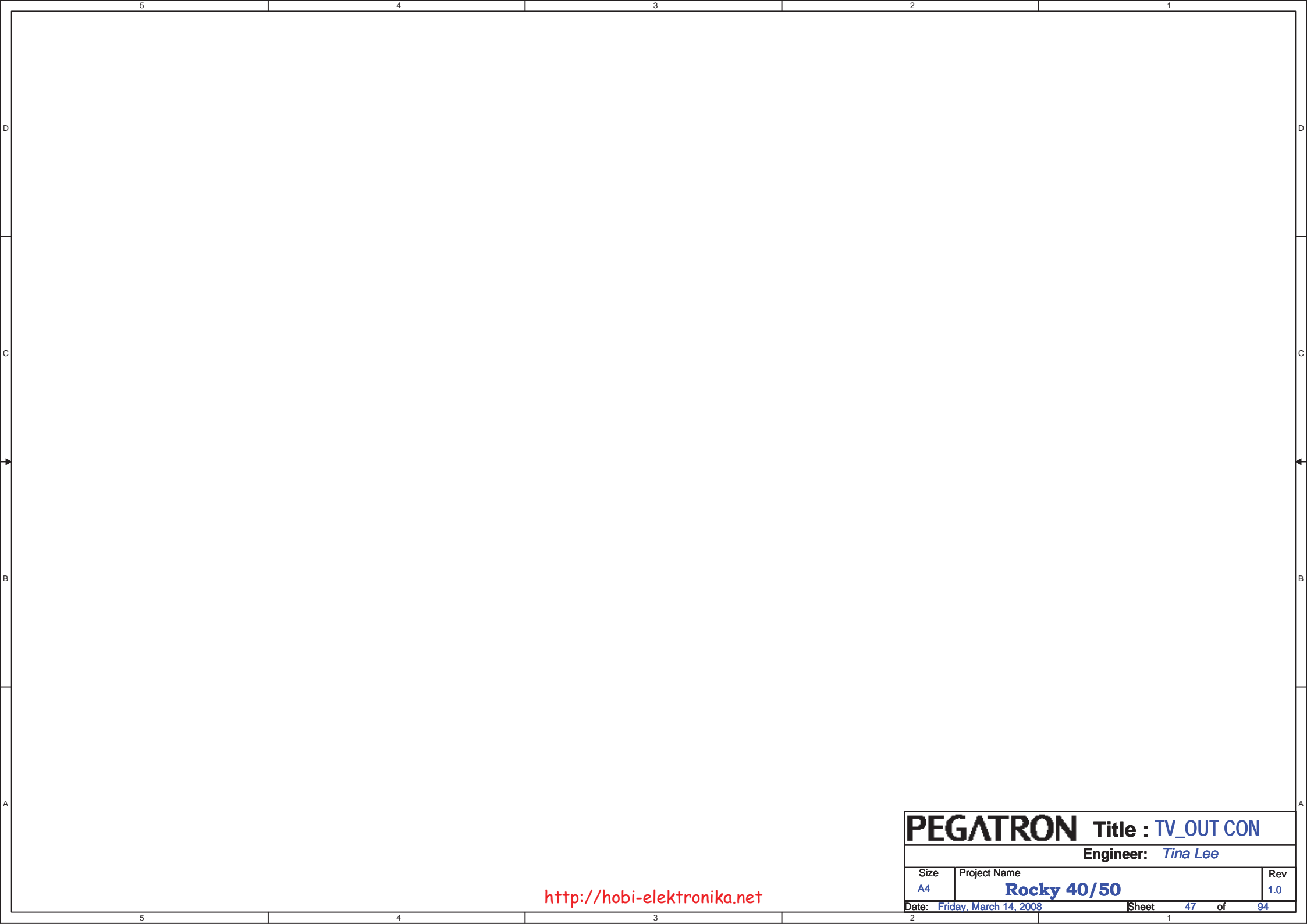


## Power Switch for LCD Power



## INVERTOR CNT





D

D

C

C

B

B

A

A

PEGATRON

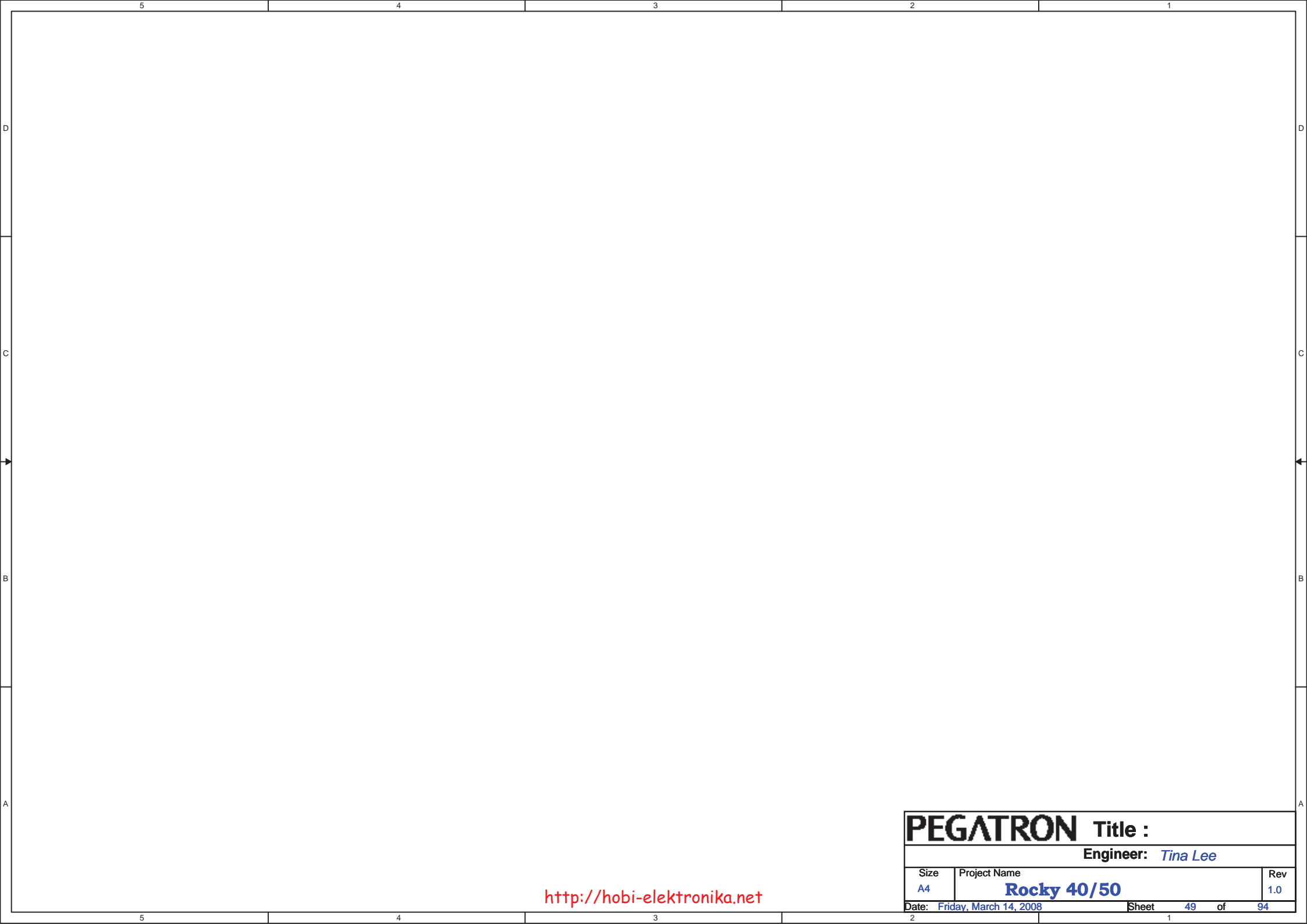
Title : TV\_OUT CON

Engineer: Tina Lee

Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008	Sheet 47 of 94	







D

C

B

A

D

C

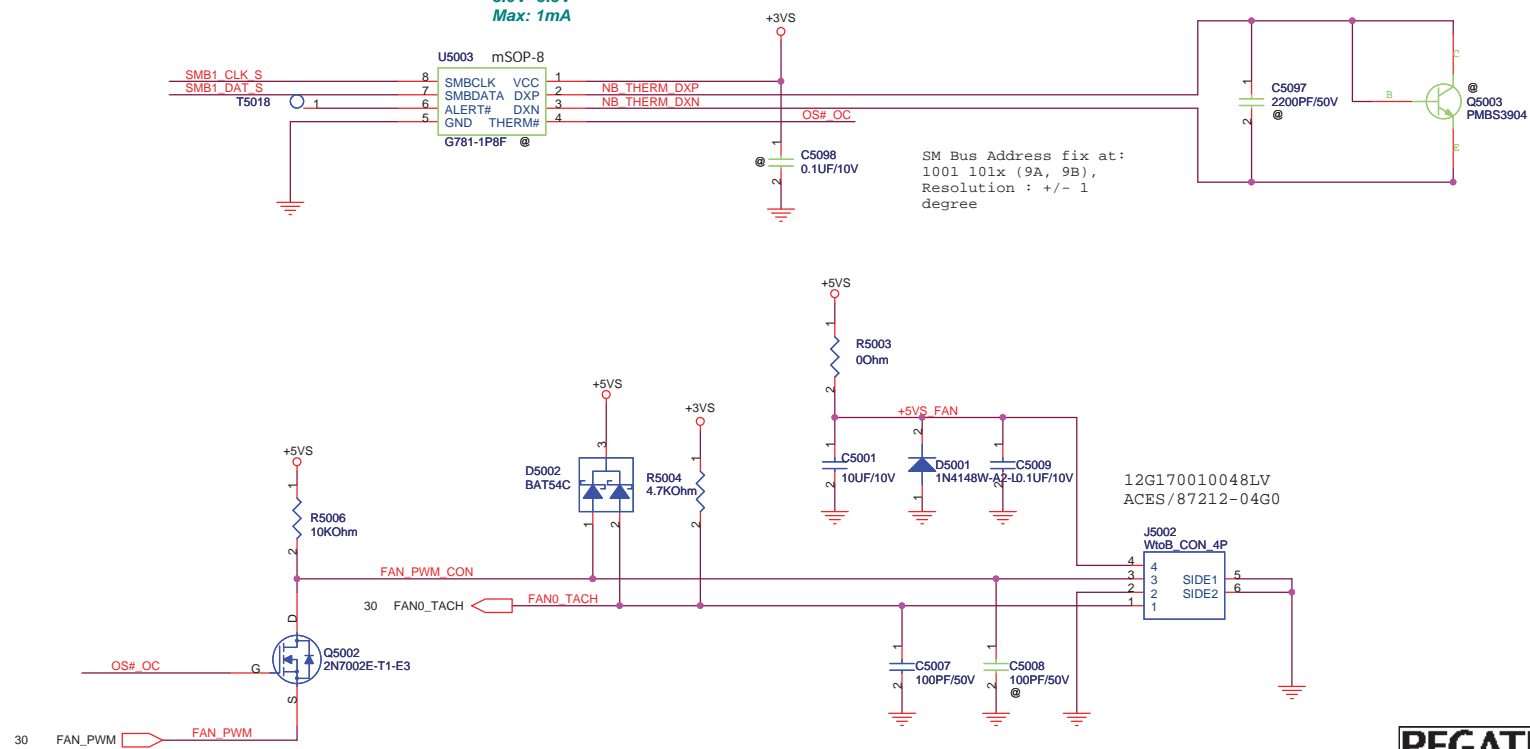
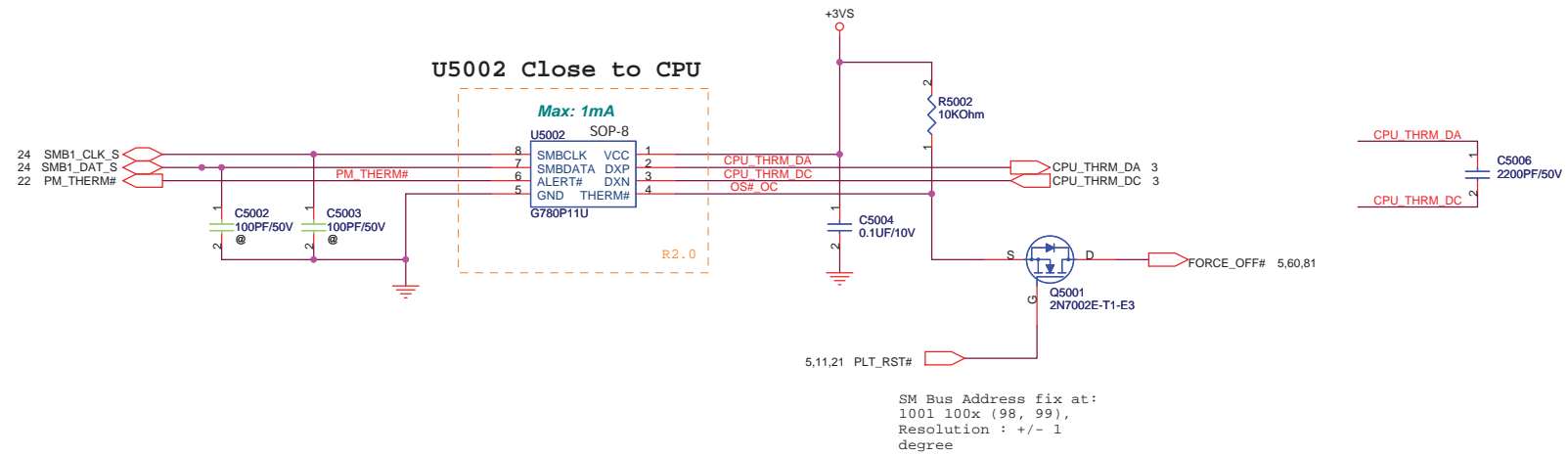
B

A

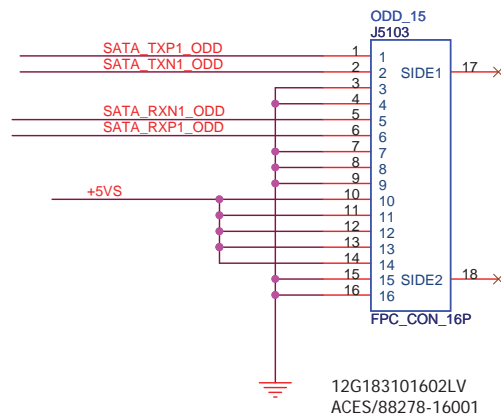
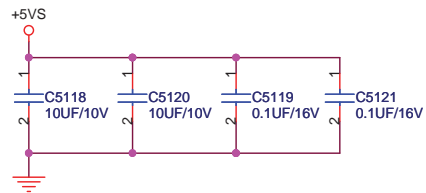
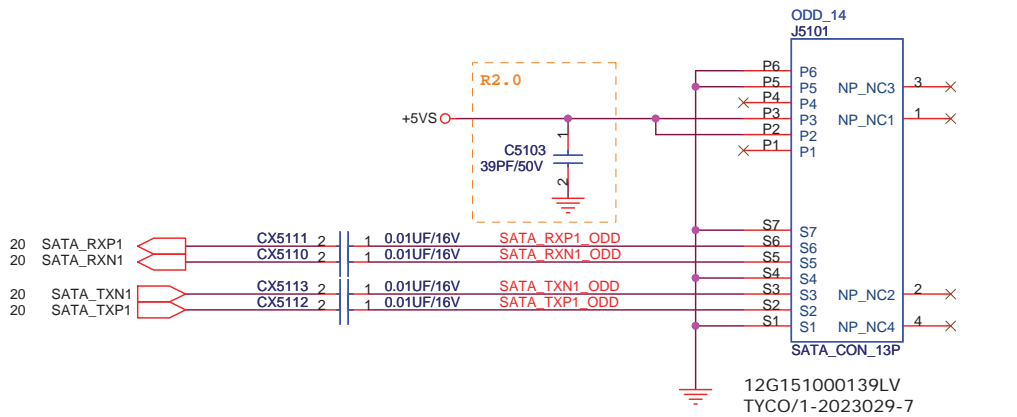
<http://hobi-elektronika.net>

PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	49	of 94

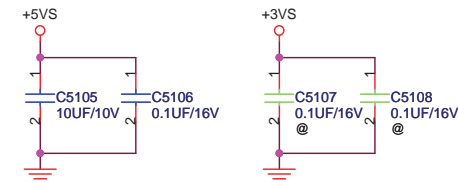
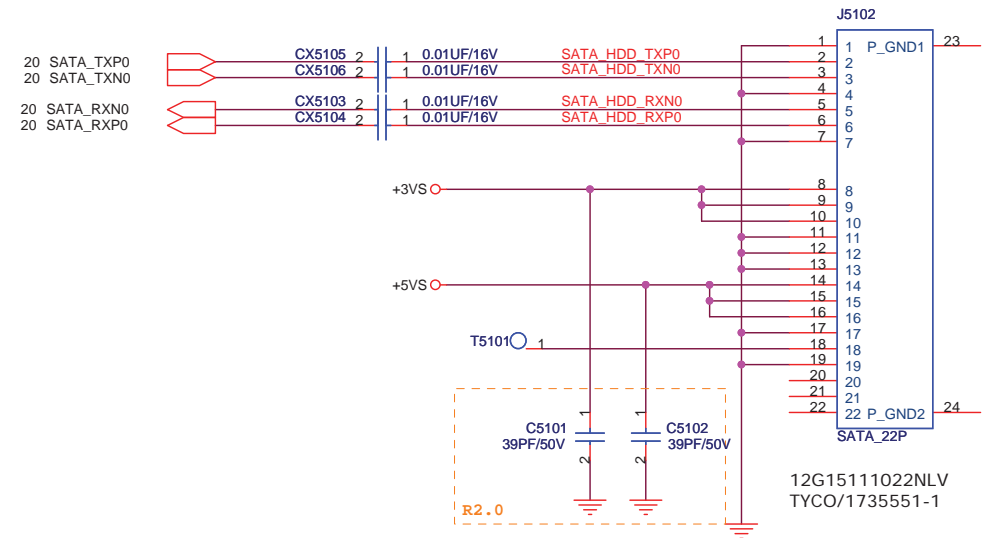
## Thermal Sensor

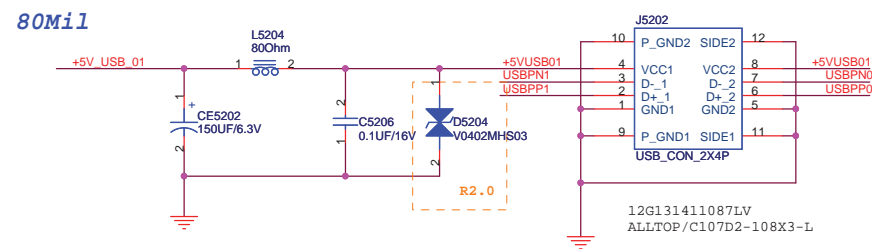
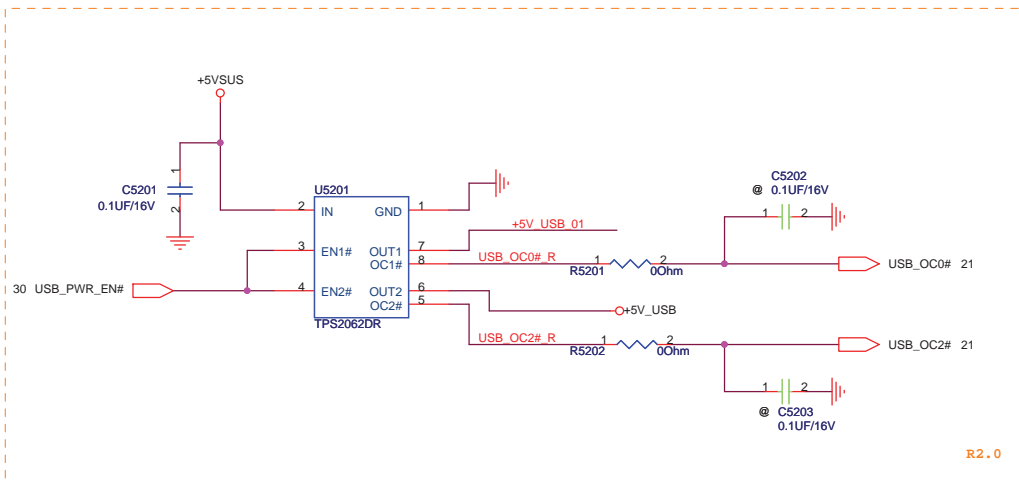
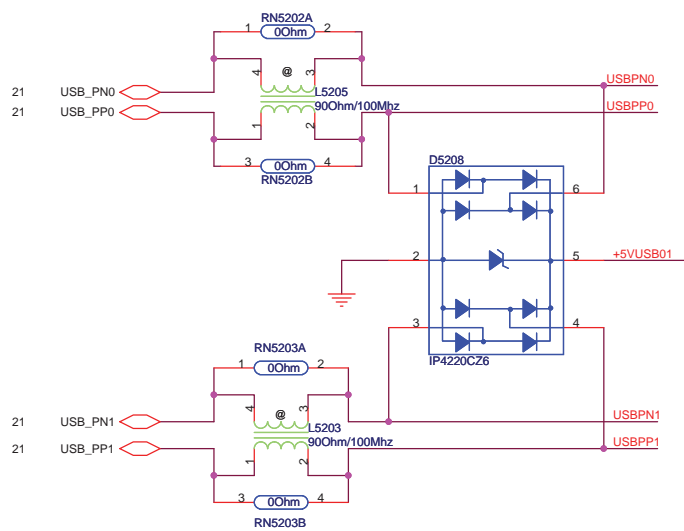


## ODD CON

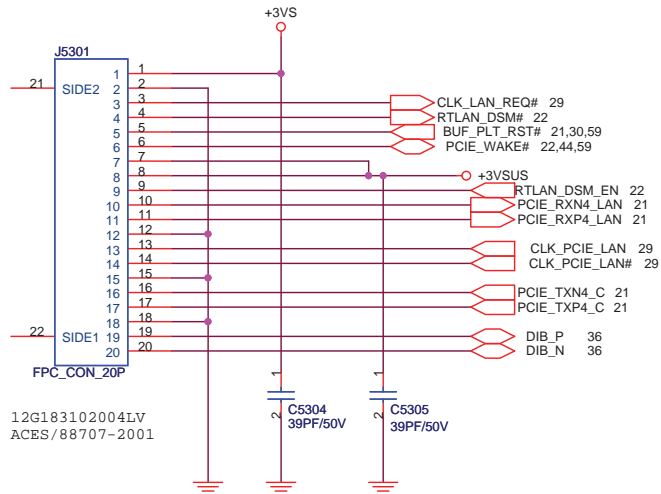


## SATA HDD CON

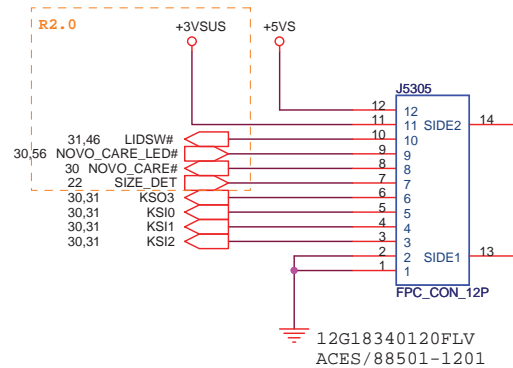




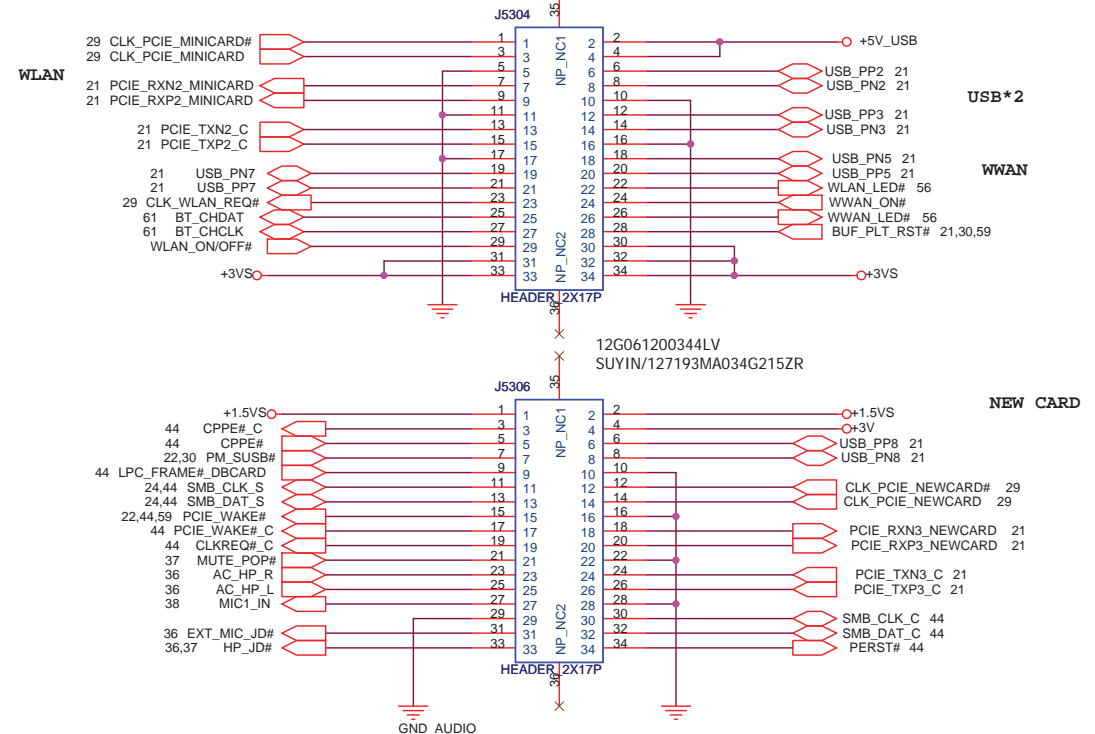
## IO BOARD



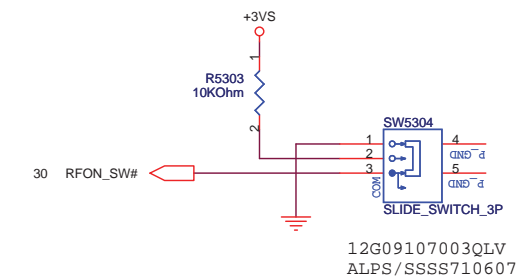
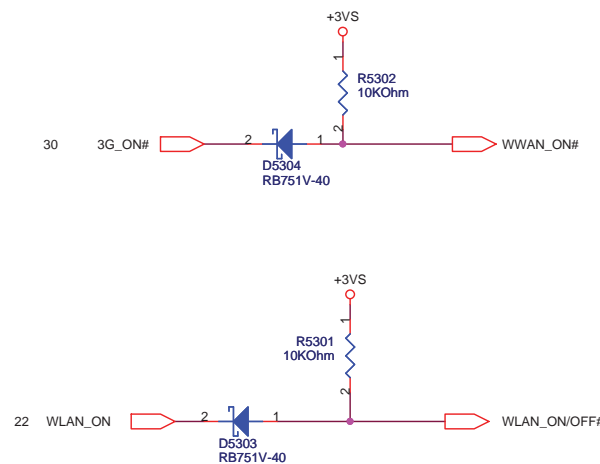
## For Media Control Board

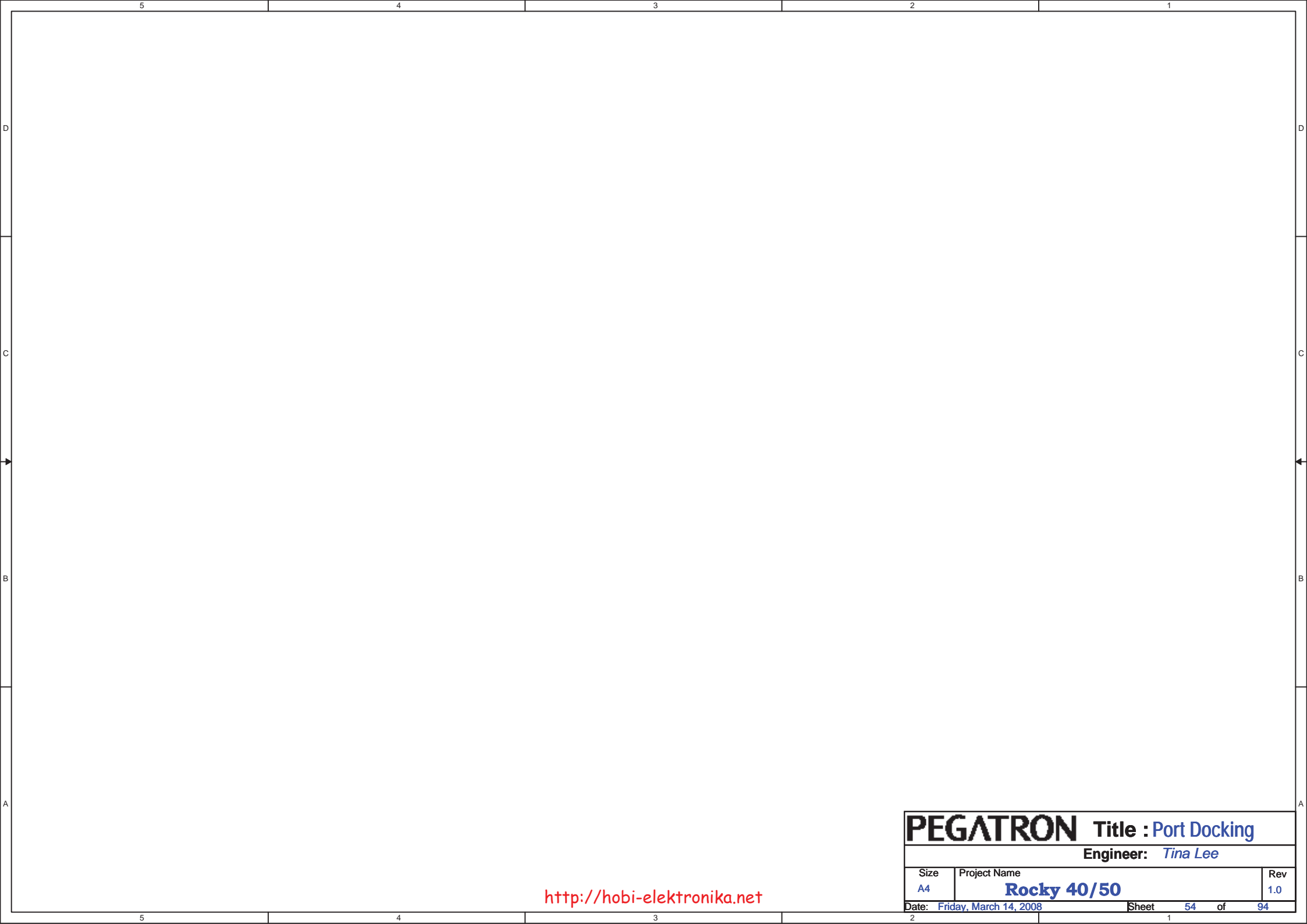


## SMALL BOARD



## Wireless Switch





D

D

C

C

B

B

A

A

<http://hobi-elektronika.net>

PEGATRON

Title : Port Docking

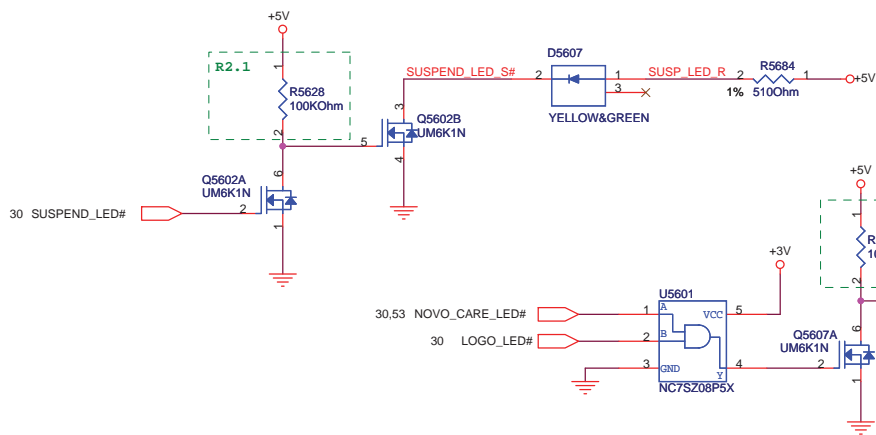
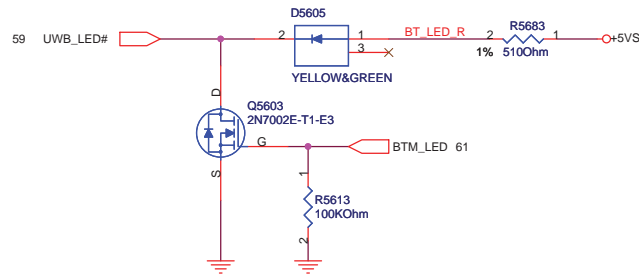
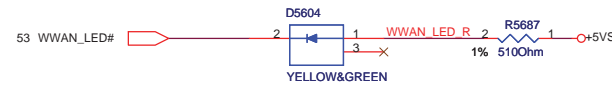
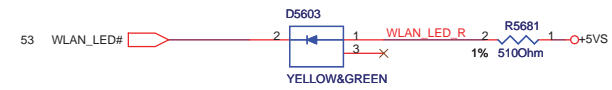
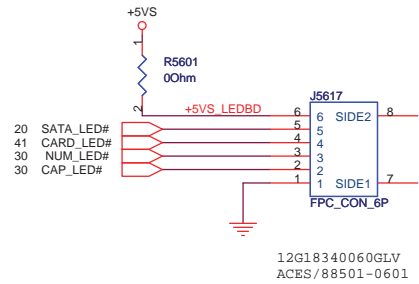
Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 54 of 94	

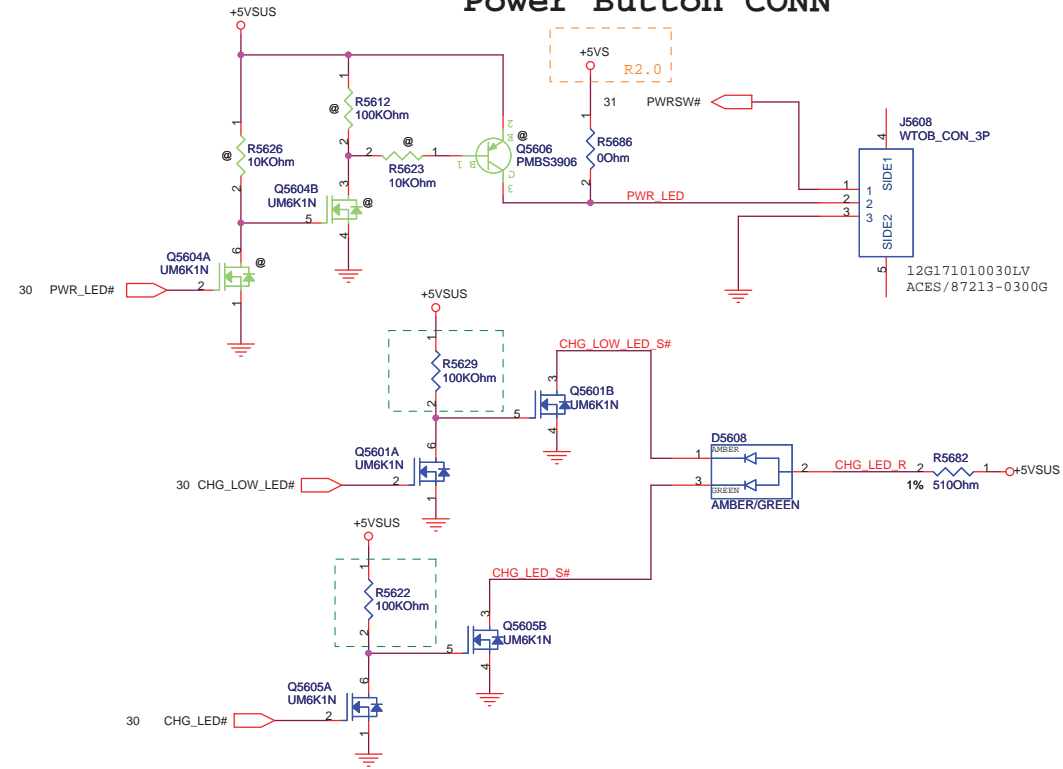
A	B	C	D	E
1				
2				
3				
4				
5				

<b>PEGATRON</b>		<b>Title :</b> <i>Super I/O &amp; FIR</i>	
<b>Engineer:</b> <i>Tina Lee</i>			
Size <i>A4</i>	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: <i>Friday, March 14, 2008</i>		Sheet	<i>55</i> of <i>94</i>

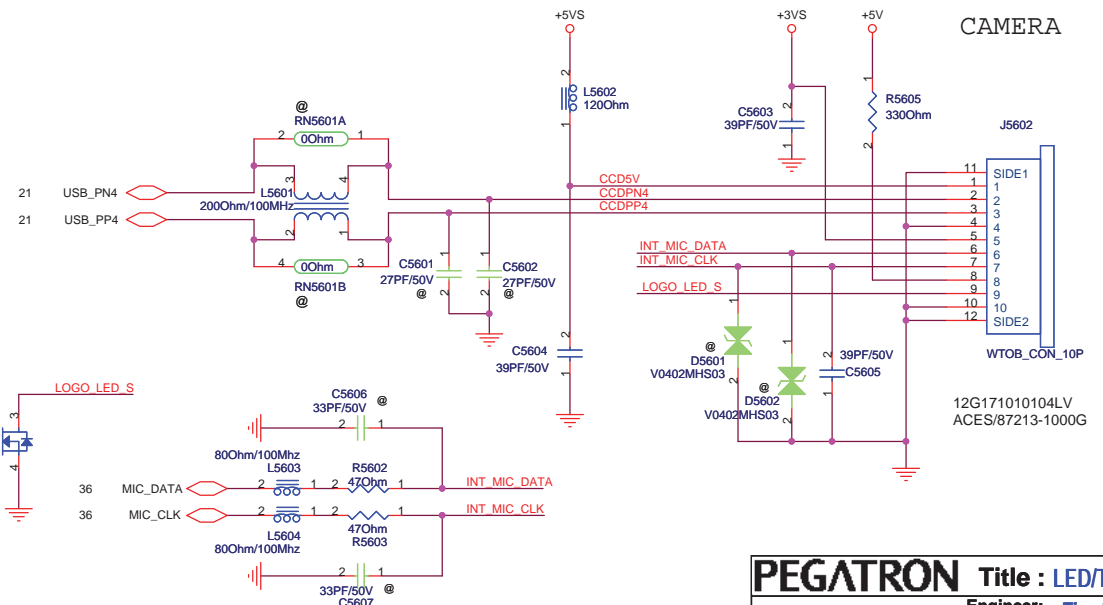
## LED CONN



## Power Button CONN



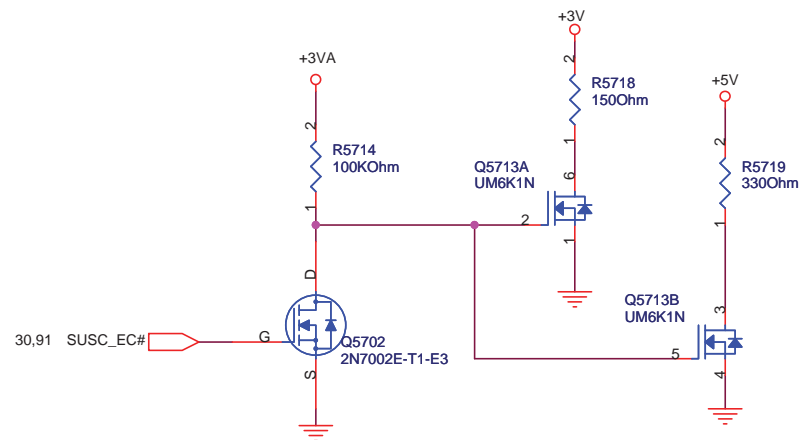
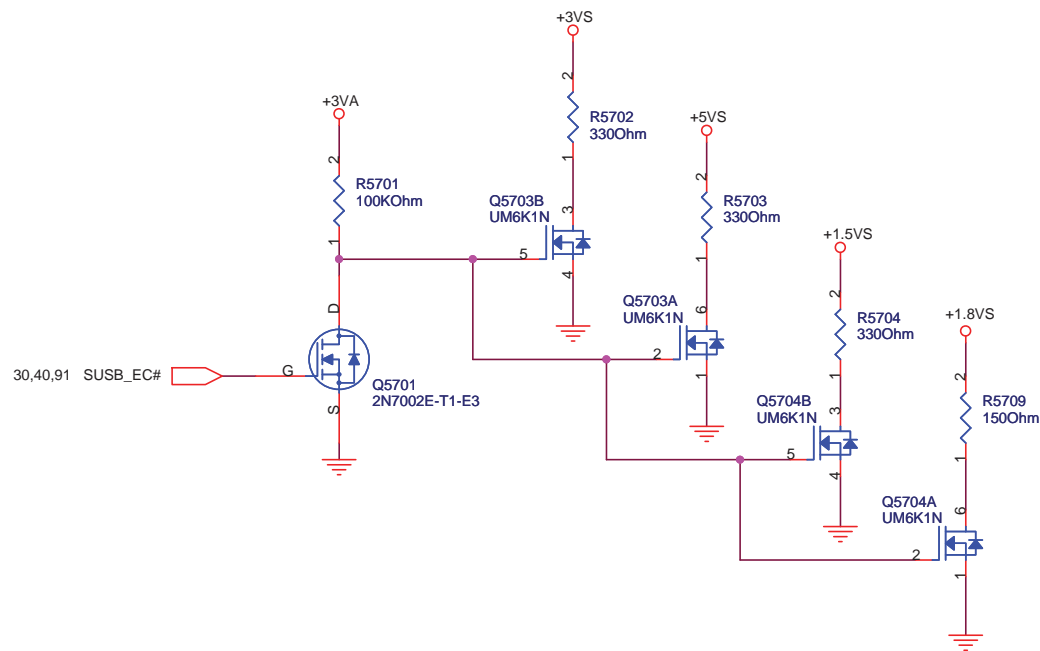
## CAMERA

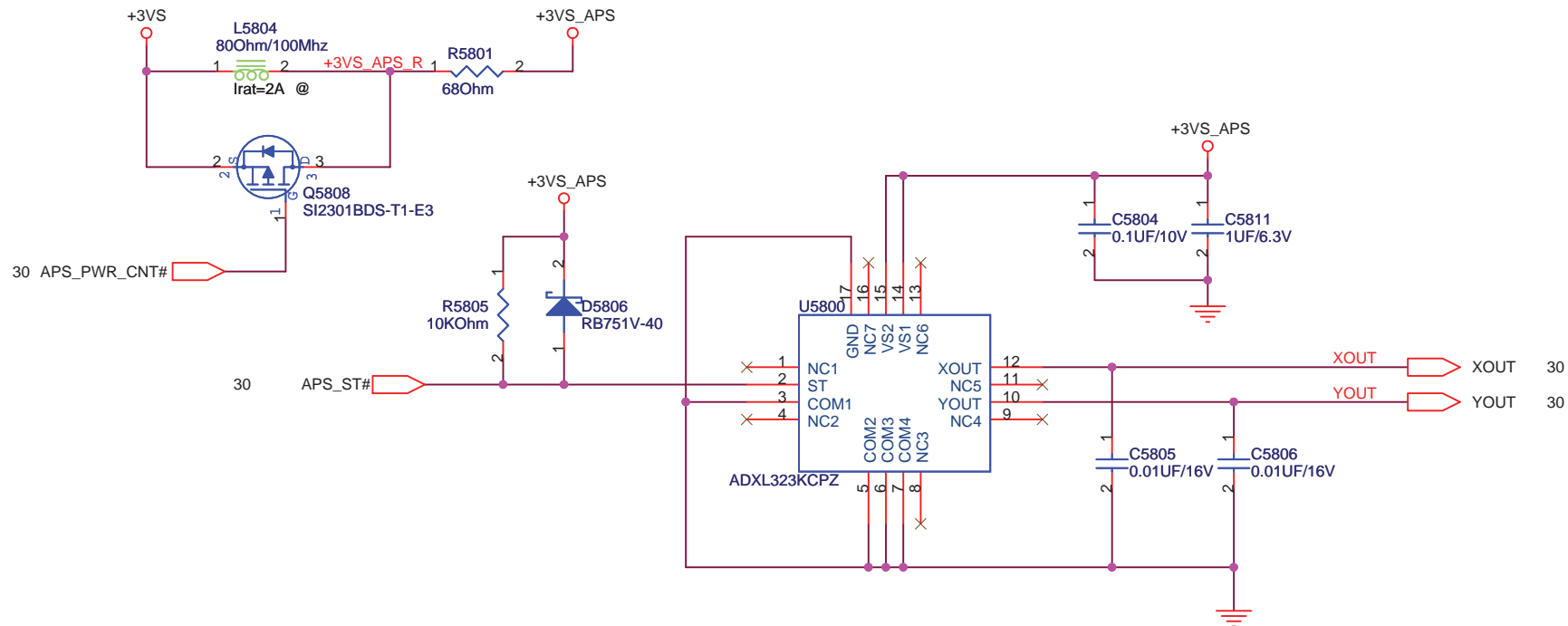


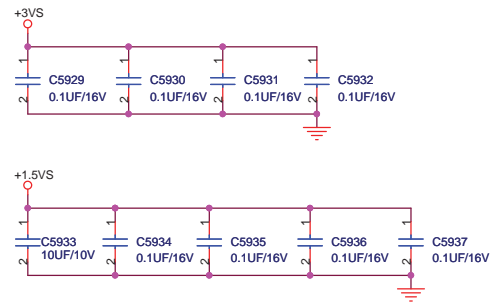
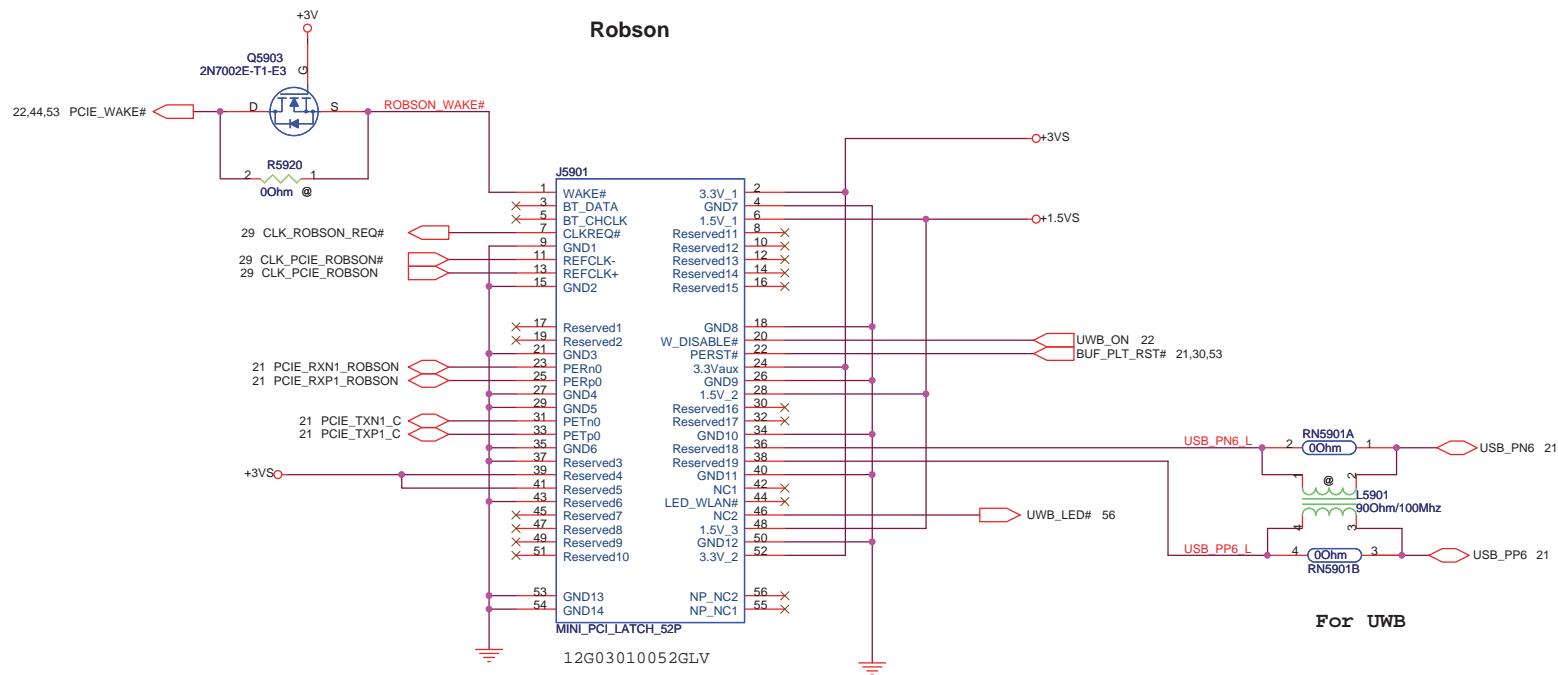
**PEGATRON** Title : LED/TP/SW  
Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0
Date: Thursday, March 27, 2008	Sheet 56 of 94	

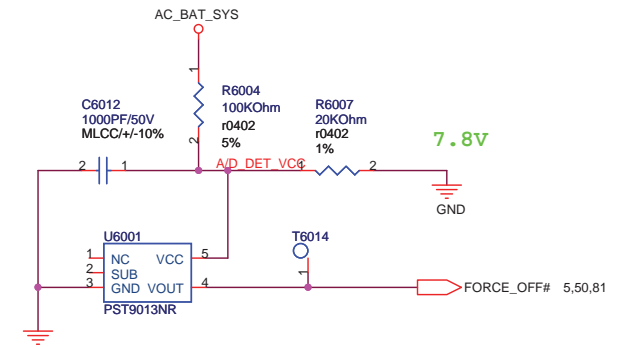
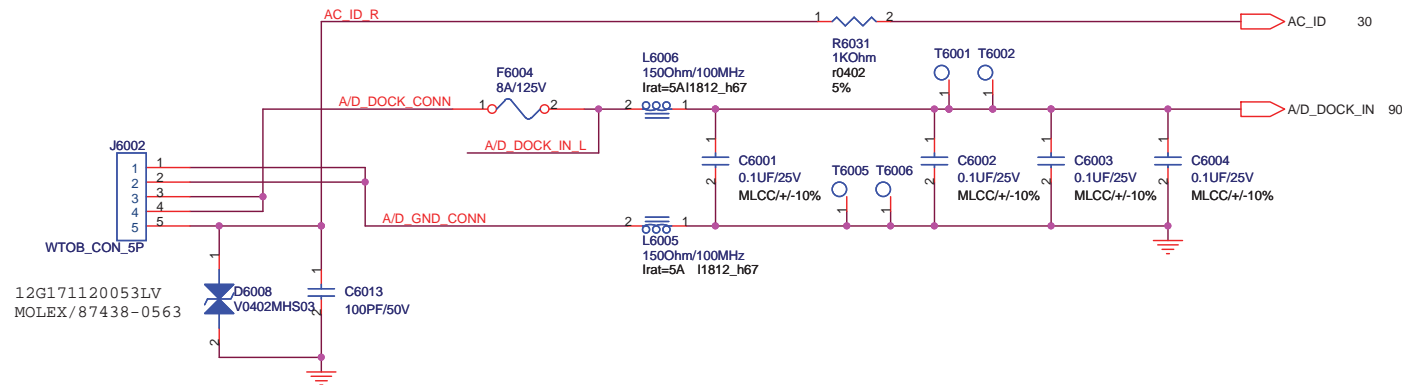






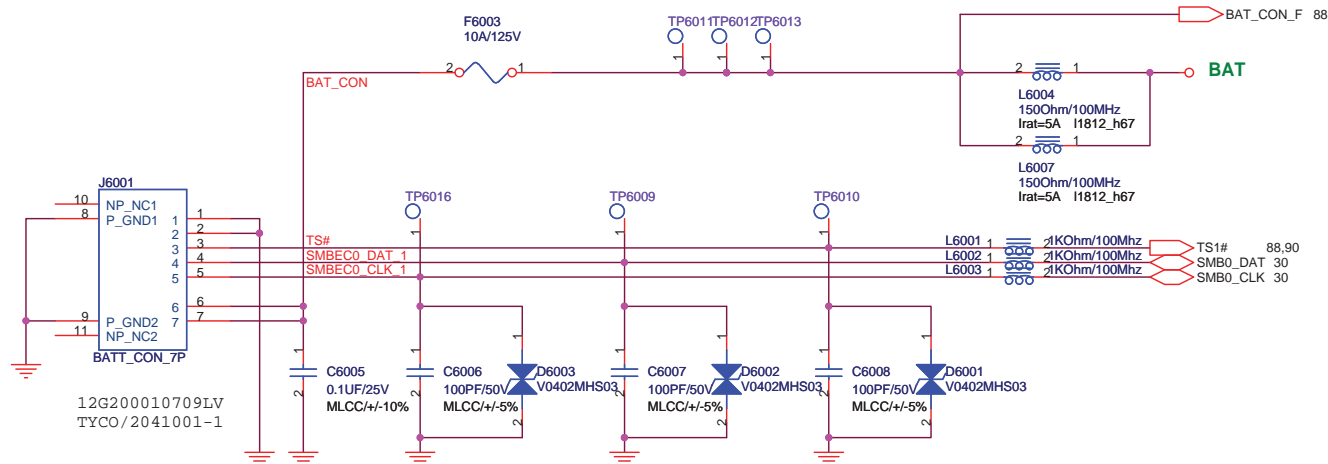


## DC IN CONN

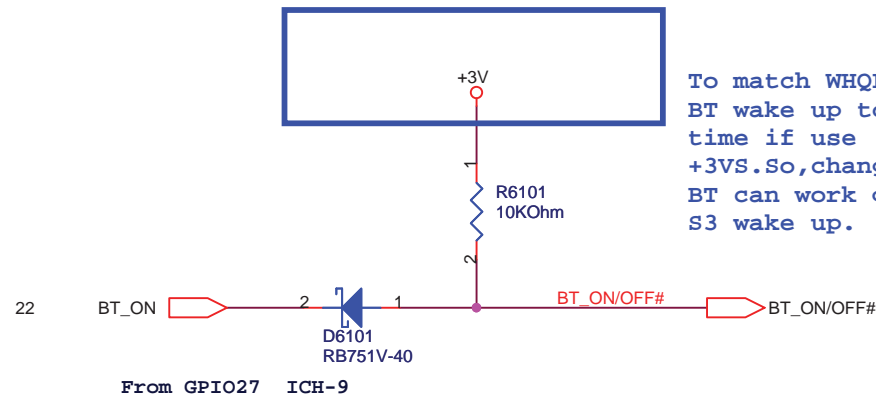
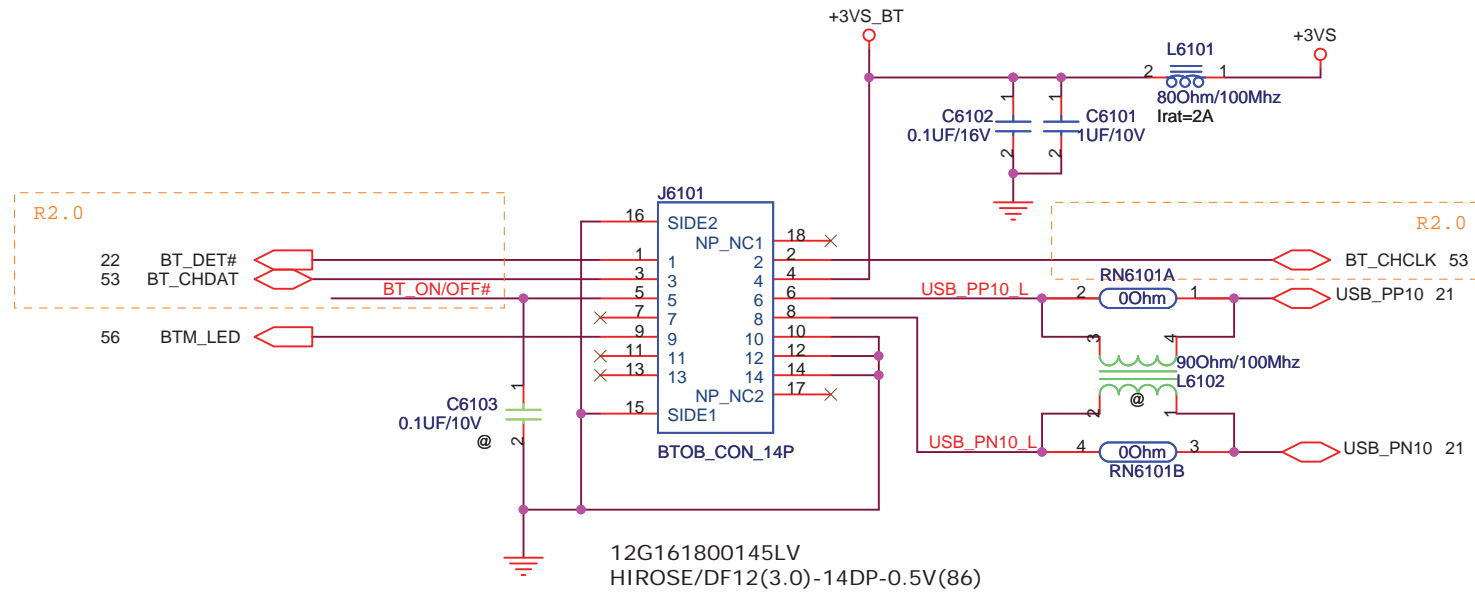


### Without Battery & Pull out Adapter

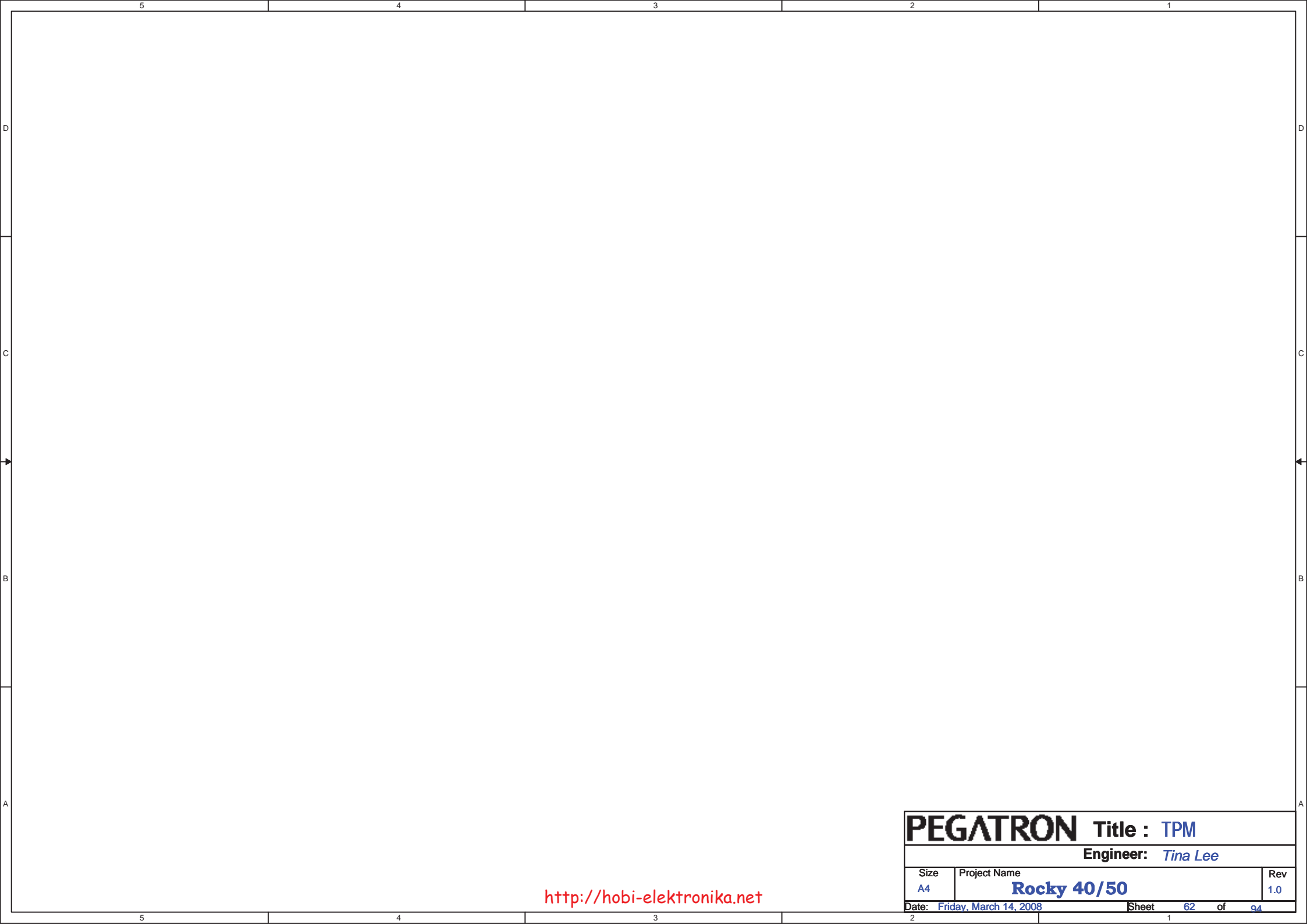
## Battery CONN



# Blue Tooth



To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.



D

C

B

A

D

C

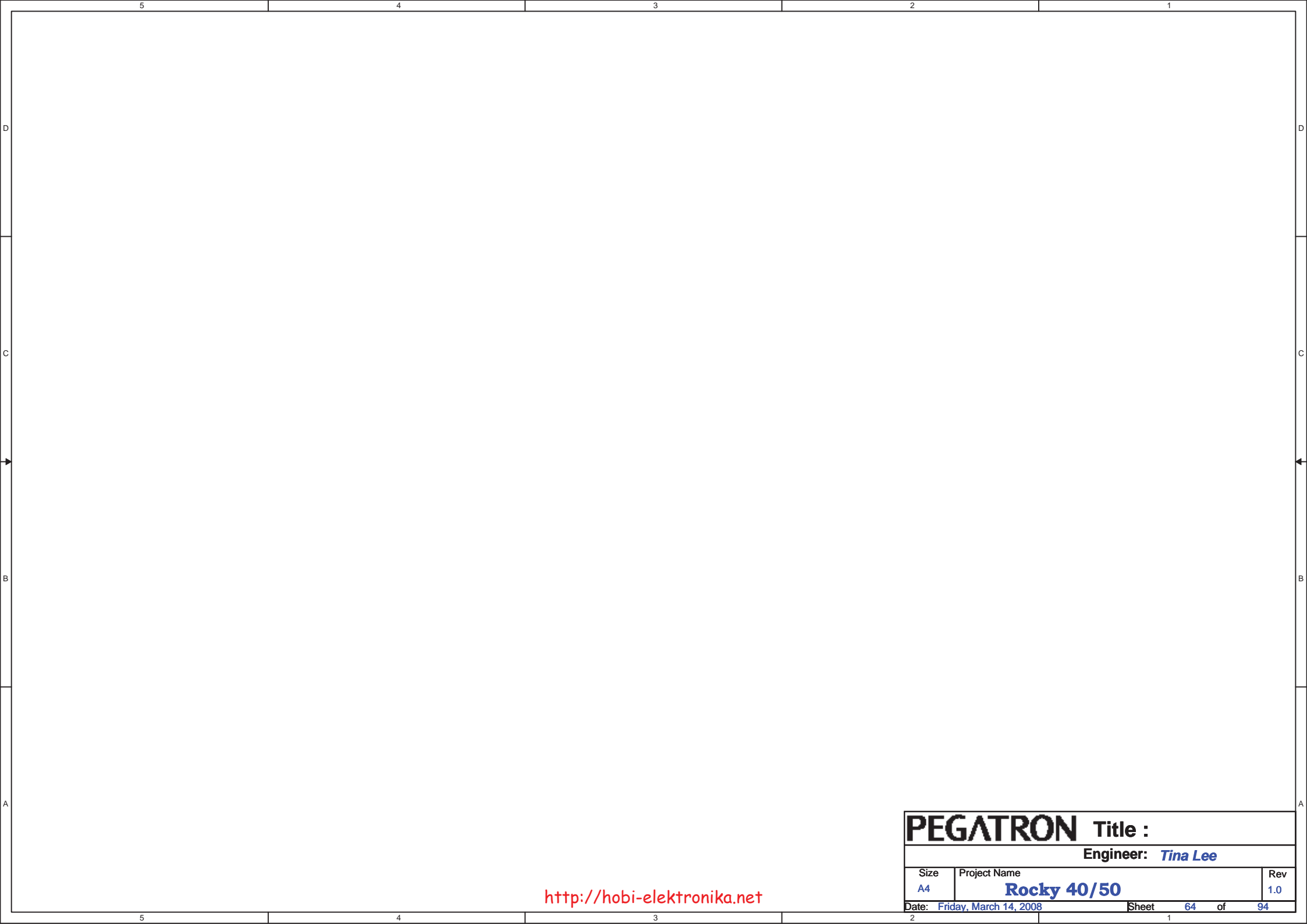
B

A

<http://hobi-elektronika.net>

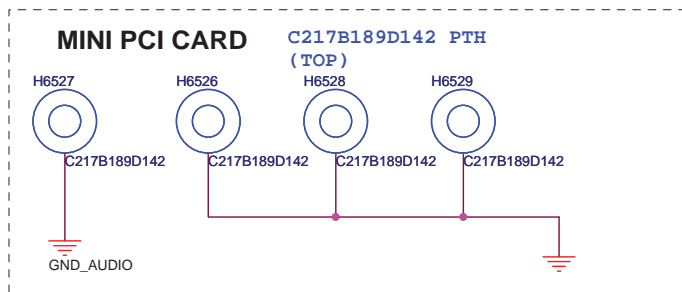
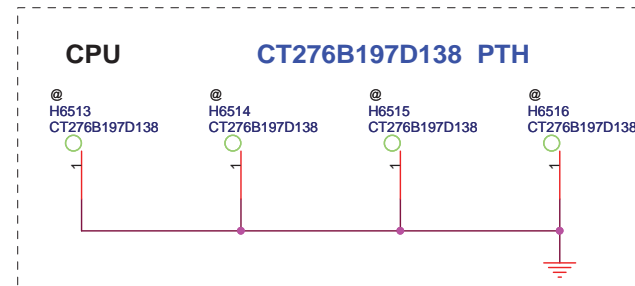
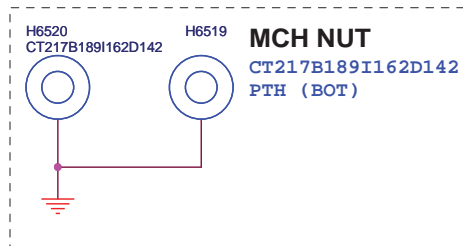
<b>PEGATRON</b>		Title : <b>TPM</b>	
Engineer: <i>Tina Lee</i>			
Size <b>A4</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>		Sheet <b>62</b> of <b>94</b>	



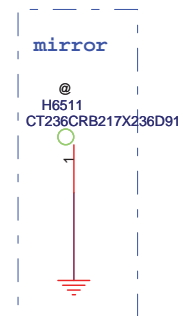
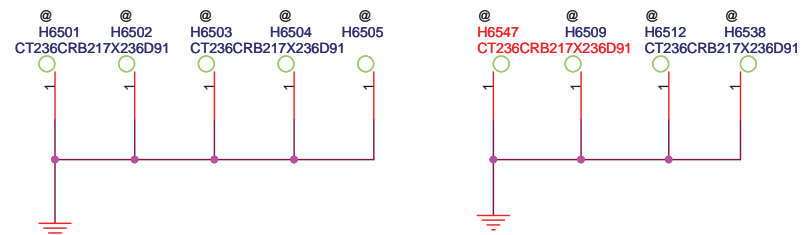


PEGATRON			Title :	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	64 of 94

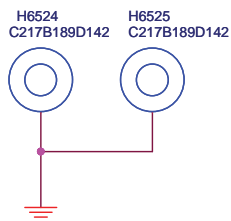




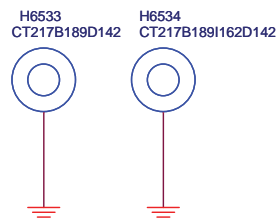
**MLB BOT - TOP SCREW HOLE**  
CT236CRB217X236D91 PTH



For Fan Stand Off  
C217B189D142 PTH (mirror/BOT)



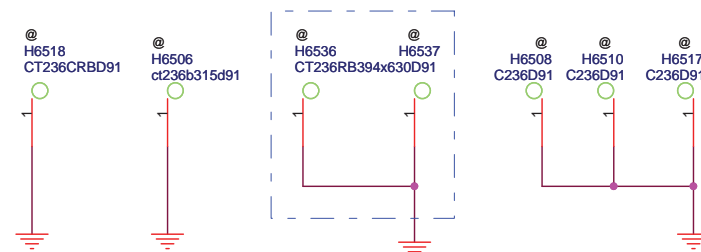
For KB Stand Off  
CT217B189D142 PTH (TOP)



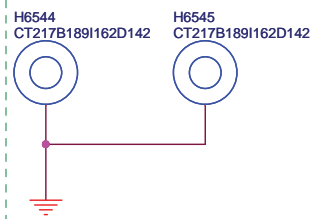
For MLB Stand Off  
CT217B236I162D142 PTH (BOT)  
H6548  
CT217B236I162D142



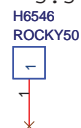
**MLB SCREW HOLE PTH**



For HDD StandOff  
(BOT)

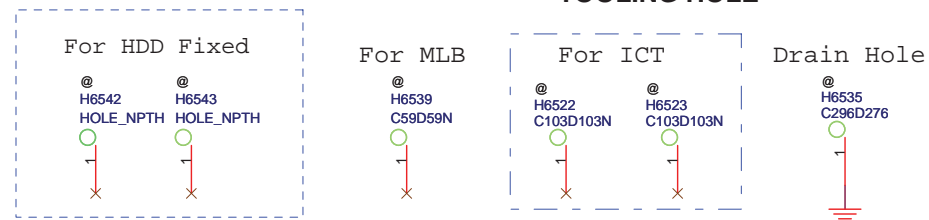


For BT StandOff  
(TOP) 5.5 PAD



R2.1

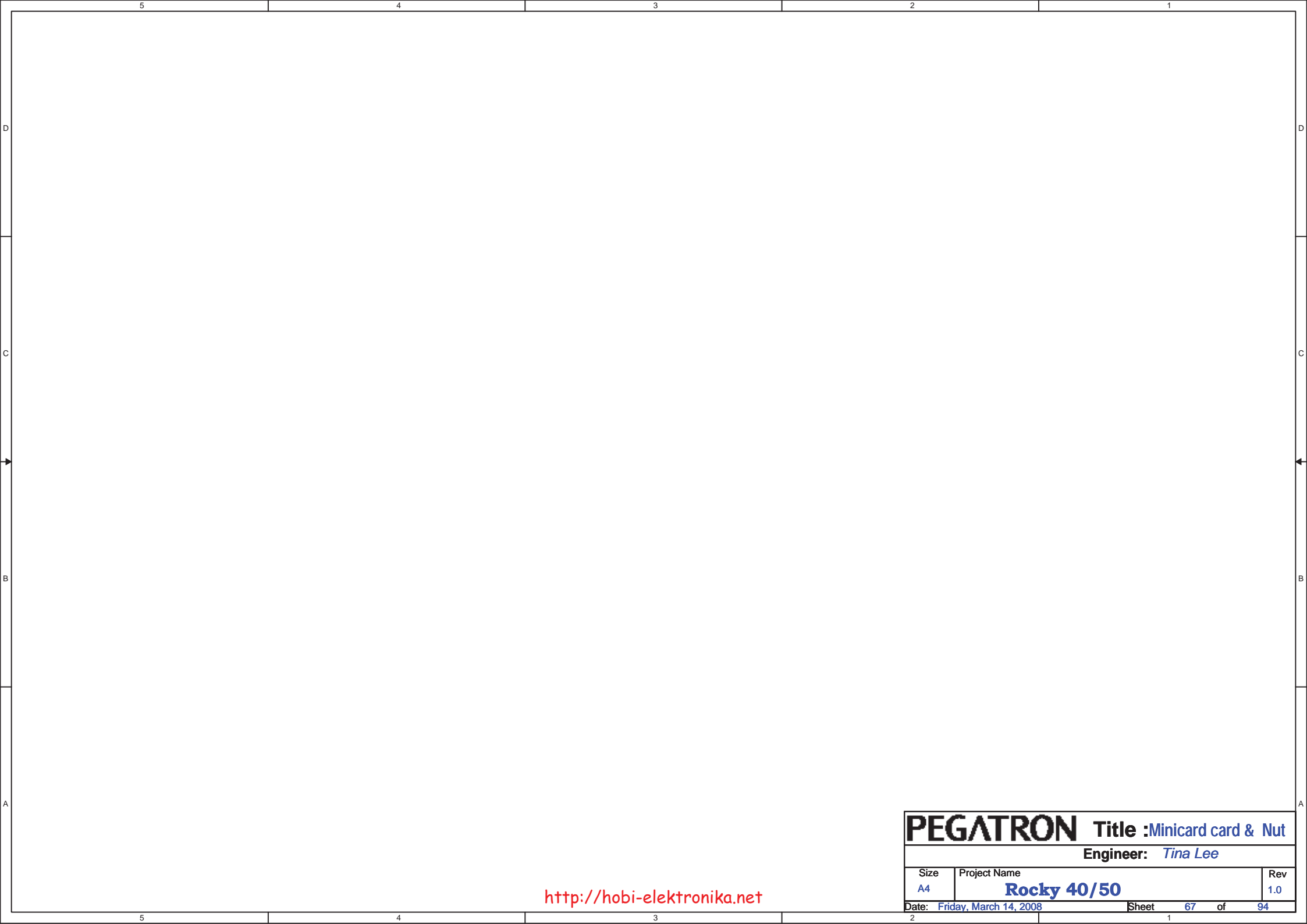
**TOOLING HOLE**



<b>PEGATRON</b>		Title MDC NUT & Hinksink NUT	
		Engineer: Tina Lee	
Size Custom	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Monday, March 24, 2008		Sheet 65	of 94

A	B	C	D	E
E				
D				
C				
B				
A				

<b>PEGATRON</b>		<b>Title : E-SATA</b>	
<b>Engineer:</b> Tina Lee			
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008		Sheet 66	of 94



D

D

C

C

B

B

A

A

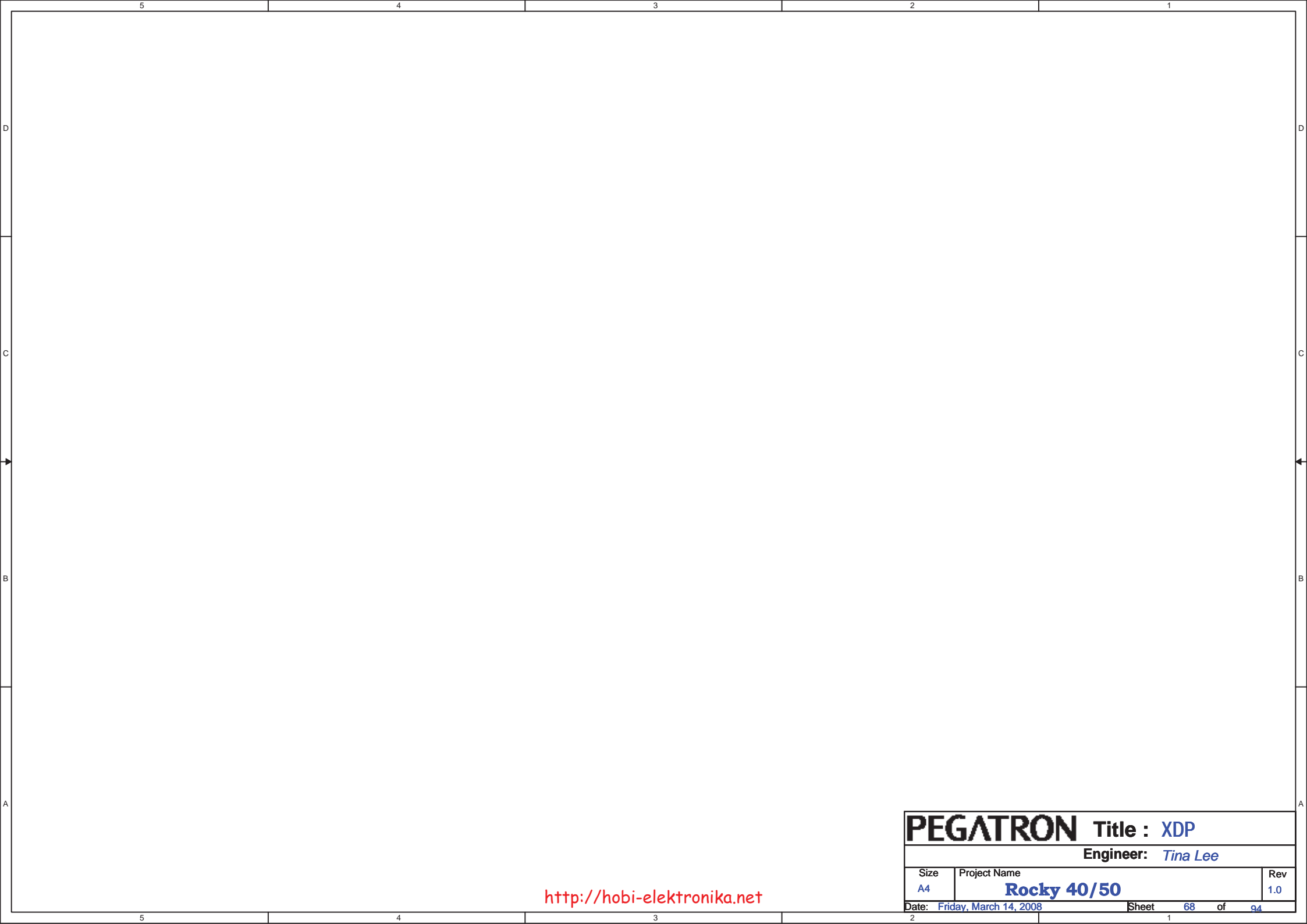
<http://hobi-elektronika.net>

PEGATRON

Title :Minicard card & Nut

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 67 of 94	



PEGATRON			Title : XDP		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	68	of 94



5	4	3	2	1
D				
C				
B				
A				

PEGATRON

Title : \*

Engineer: Tina Lee

Size A4	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Friday, March 14, 2008	Sheet 70 of 94	

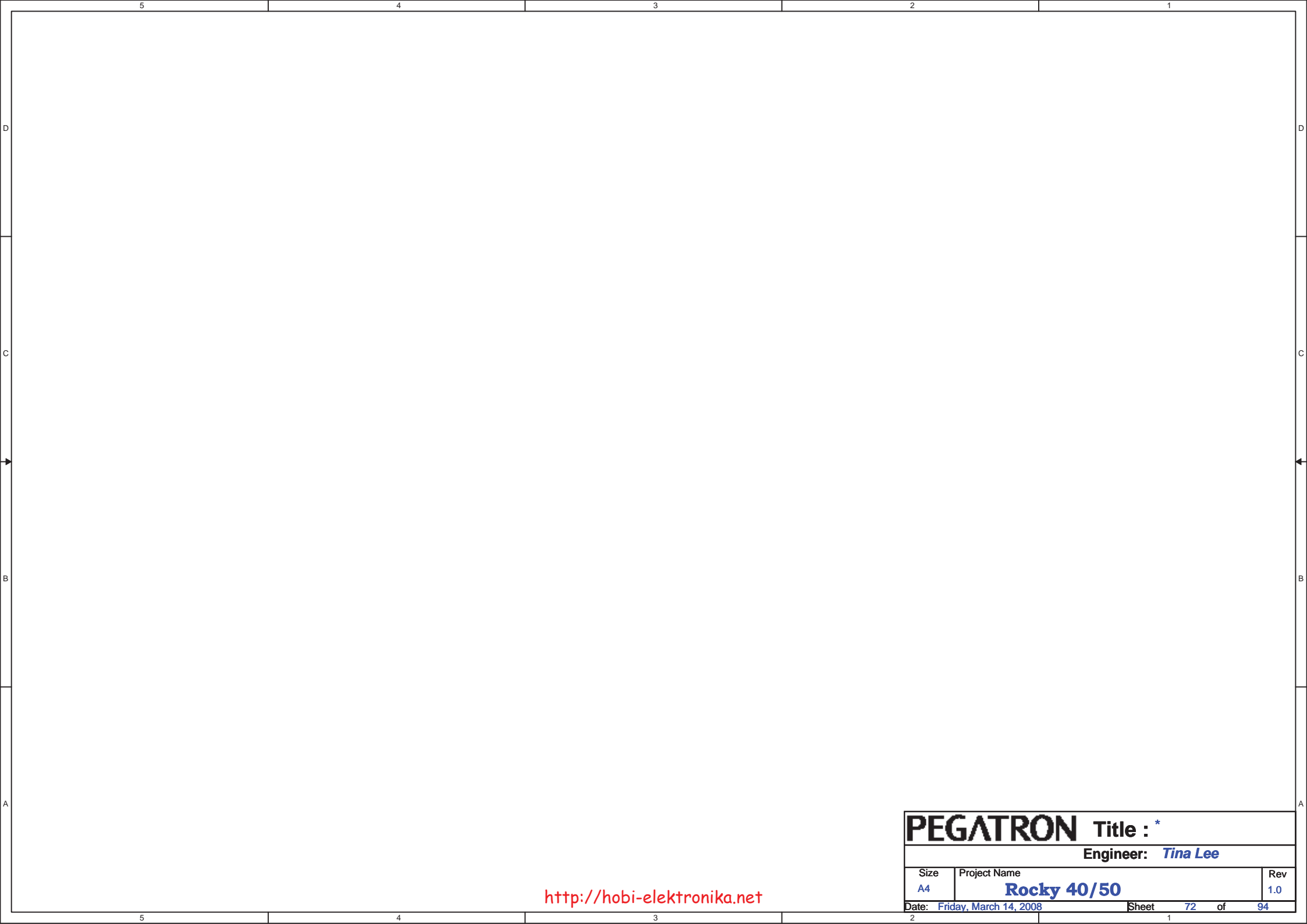
5	4	3	2	1
D				
C				
B				
A				

PEGATRON

Title : \*

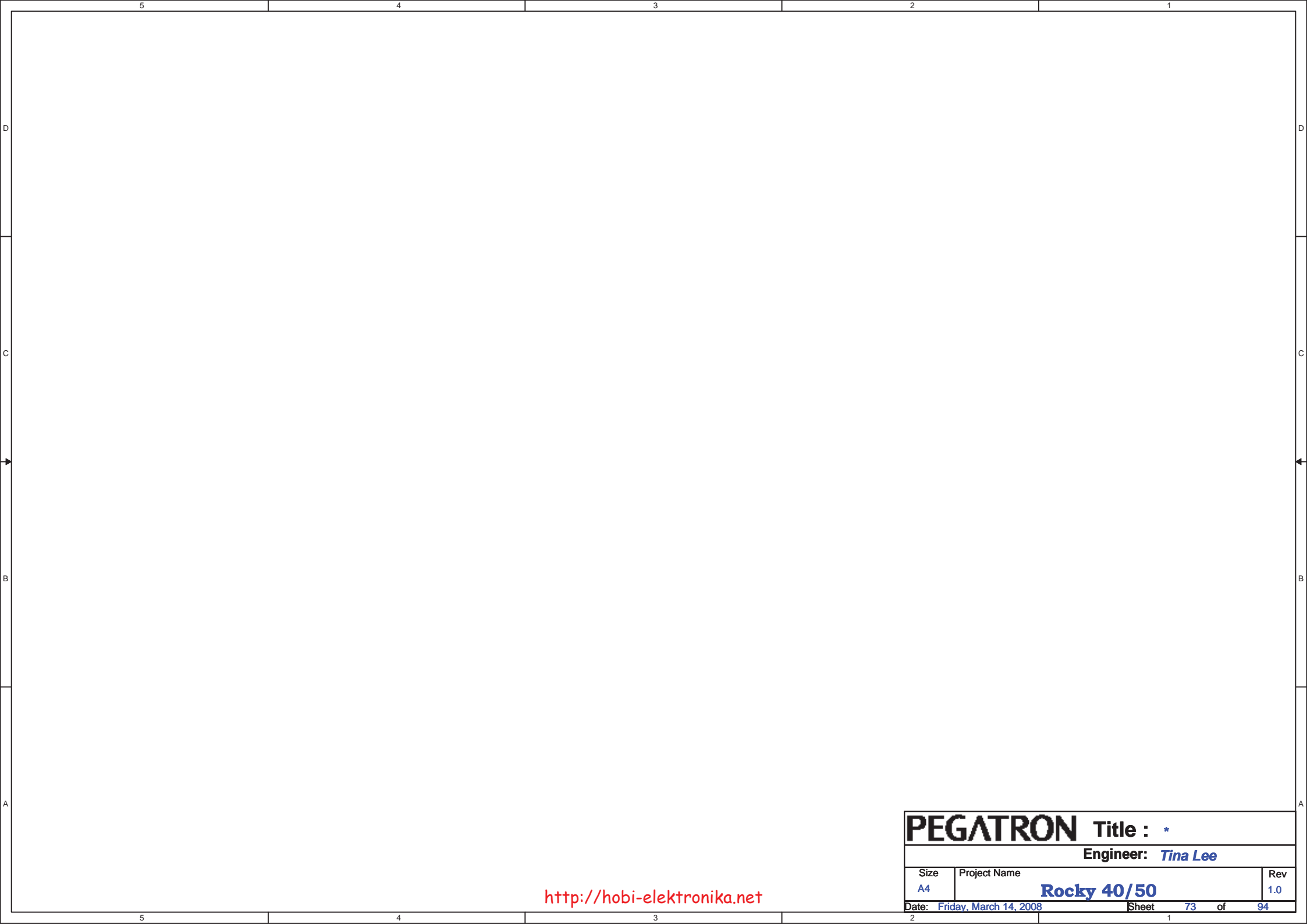
Engineer: Tina Lee

Size A4	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Friday, March 14, 2008	Sheet 71	of 94



PEGATRON			Title : *		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	72	of 94



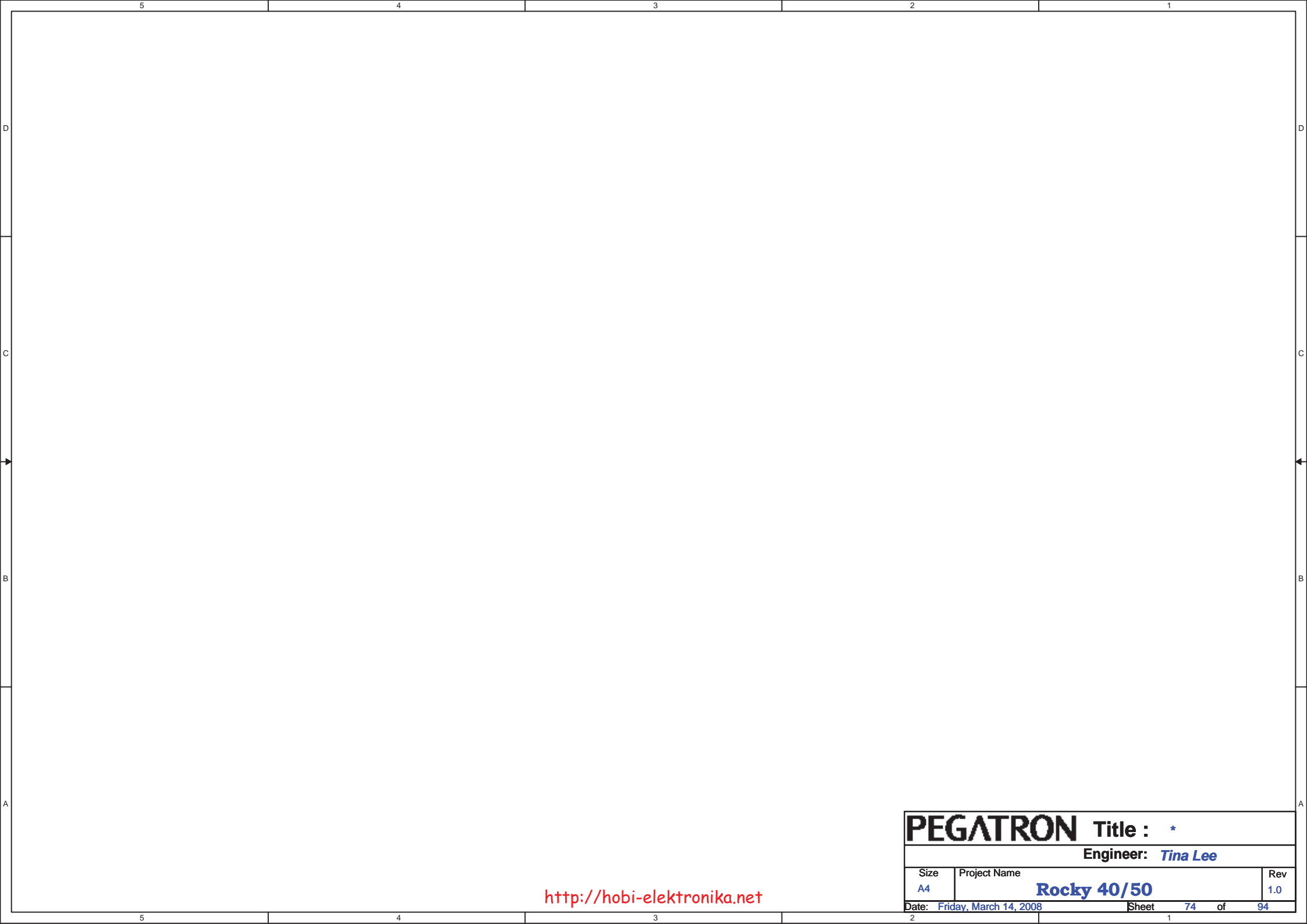


PEGATRON

Title : \*

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 73 of 94	



D

C

B

A

D

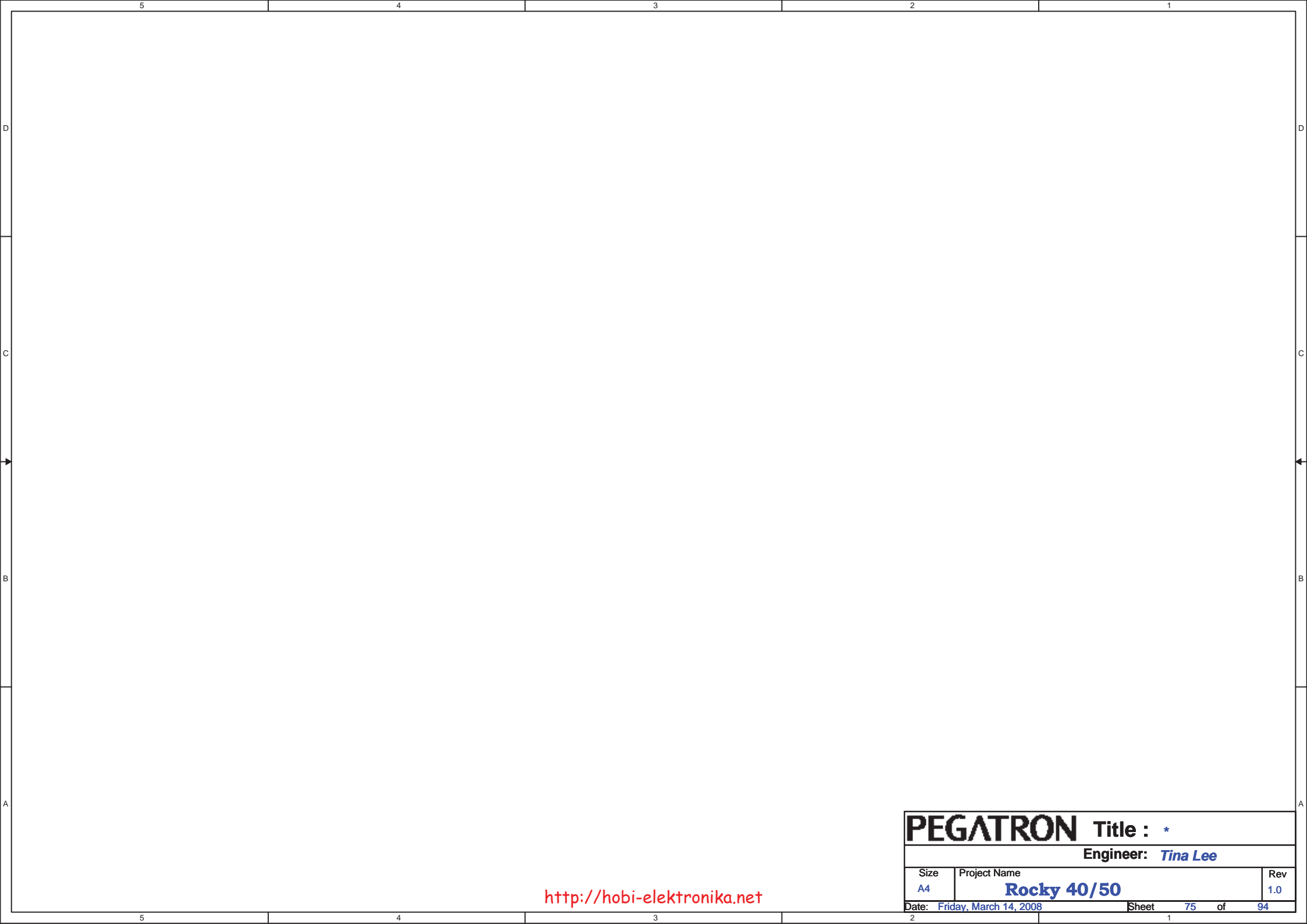
C

B

A

<http://hobi-elektronika.net>

<b>PEGATRON</b>		Title : *	
Engineer: <i>Tina Lee</i>			
Size <b>A4</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>	Sheet <b>74</b> of <b>94</b>		



D

C

B

A

D

C

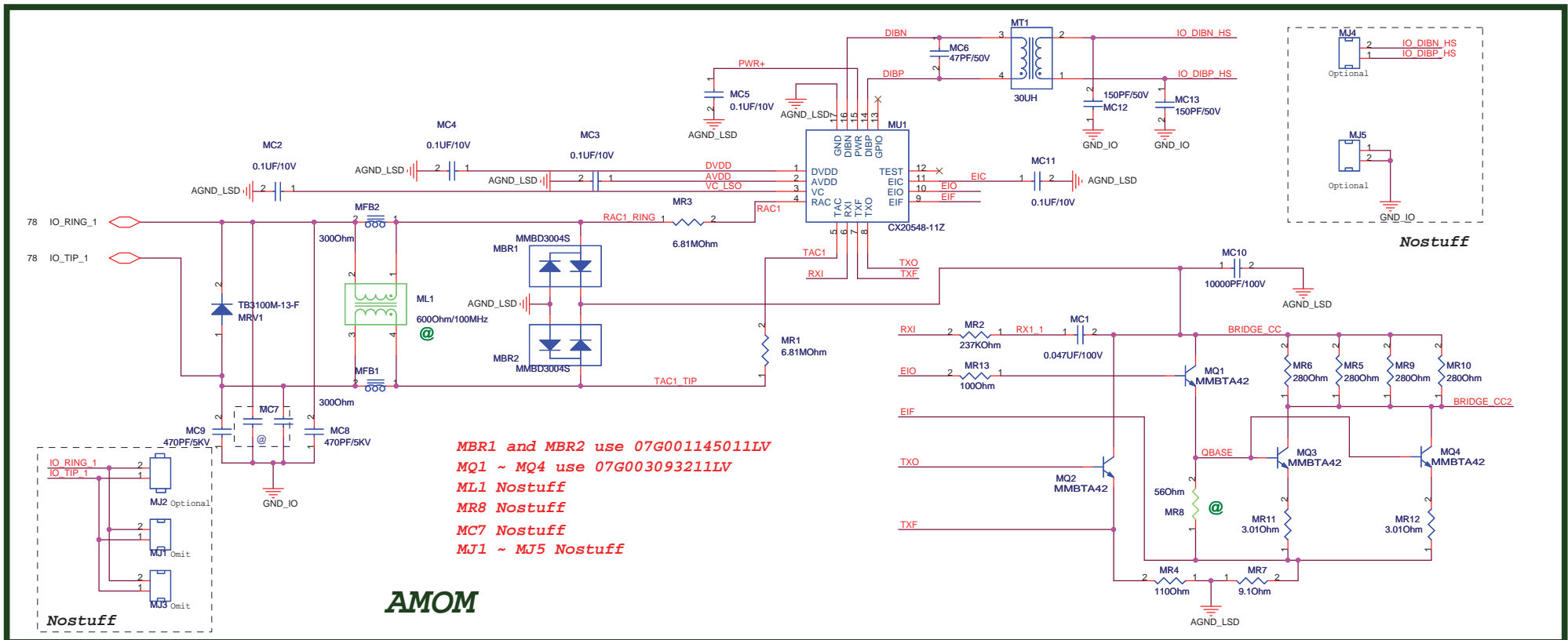
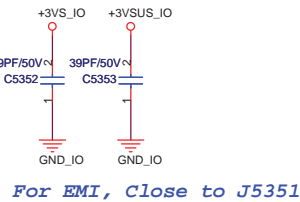
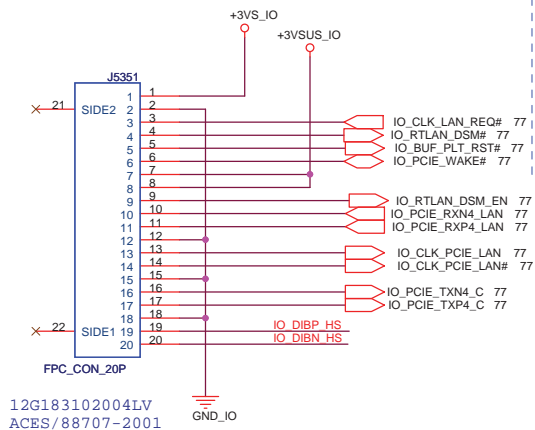
B

A

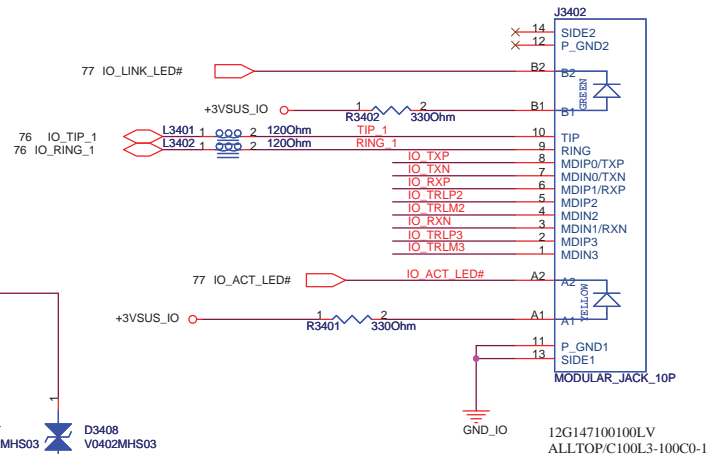
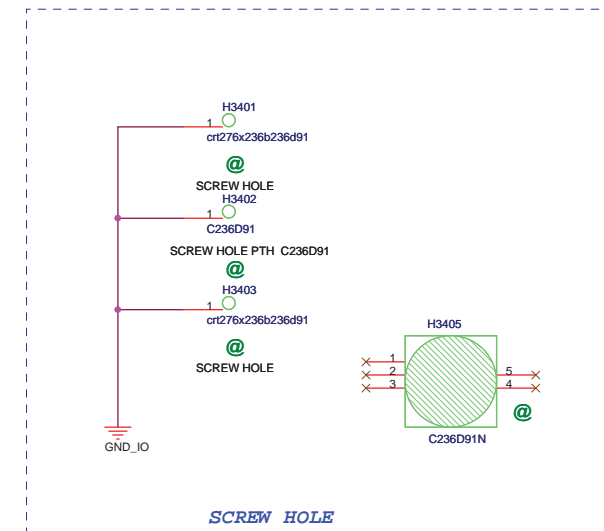
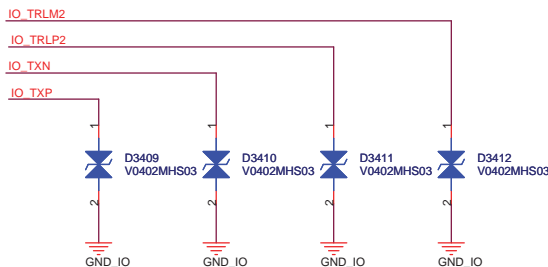
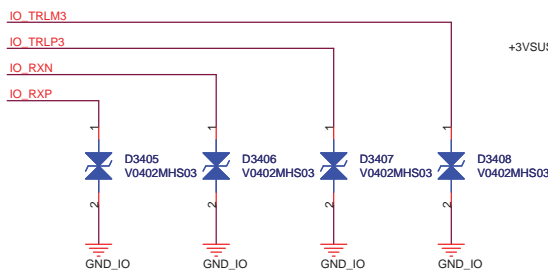
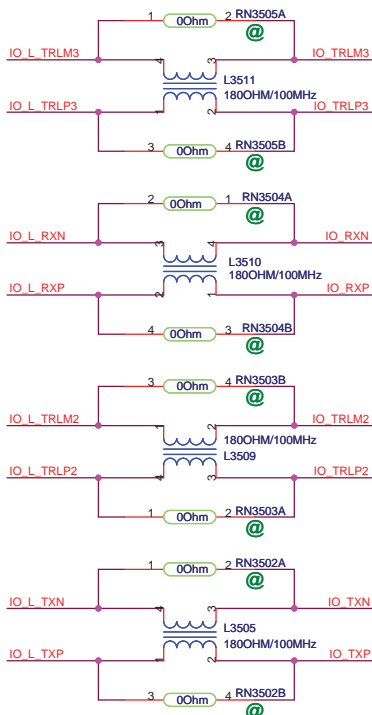
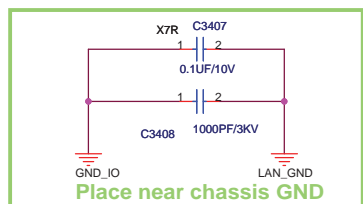
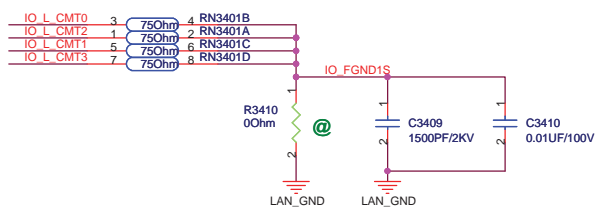
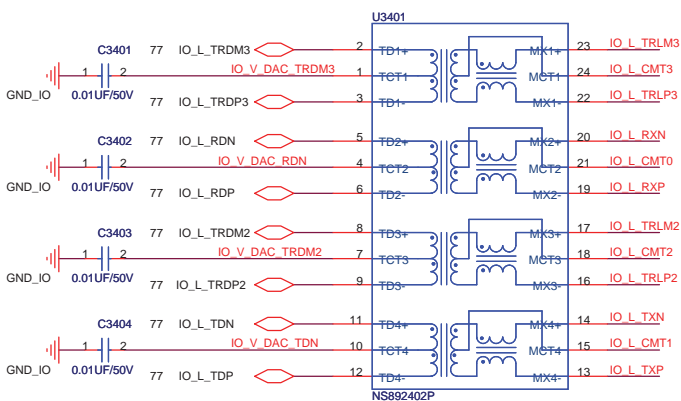
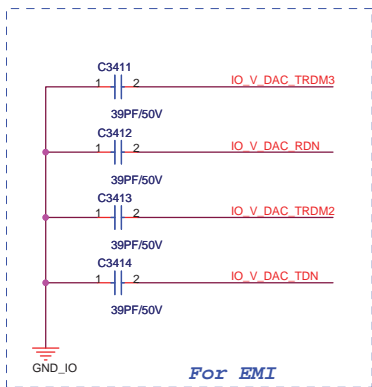
<http://hobi-elektronika.net>

PEGATRON		Title : *	
		Engineer: <i>Tina Lee</i>	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date:	Friday, March 14, 2008	Sheet	75 of 94

# IO BOARD







<Variant Name>

<b>ASUS</b>		Title : LAN-RJ45	
ASUSTek COMPUTER INC		Engineer: Warren	
Size Custom	Project Name Rocky 50 IO Board	Rev 2.0	
Date: Thursday, March 27, 2008		Sheet 78 of 94	

D

C

B

A

1

2

3

4

5

D

C

B

A

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1

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2

3

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4

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5

**PEGATRON** Title : **History**

**Engineer:** *Tina Lee*

Size	Project Name	Rev
A	<b>Rocky 40/50</b>	1.0

Date: Friday, March 14, 2008 Sheet 79 of 94

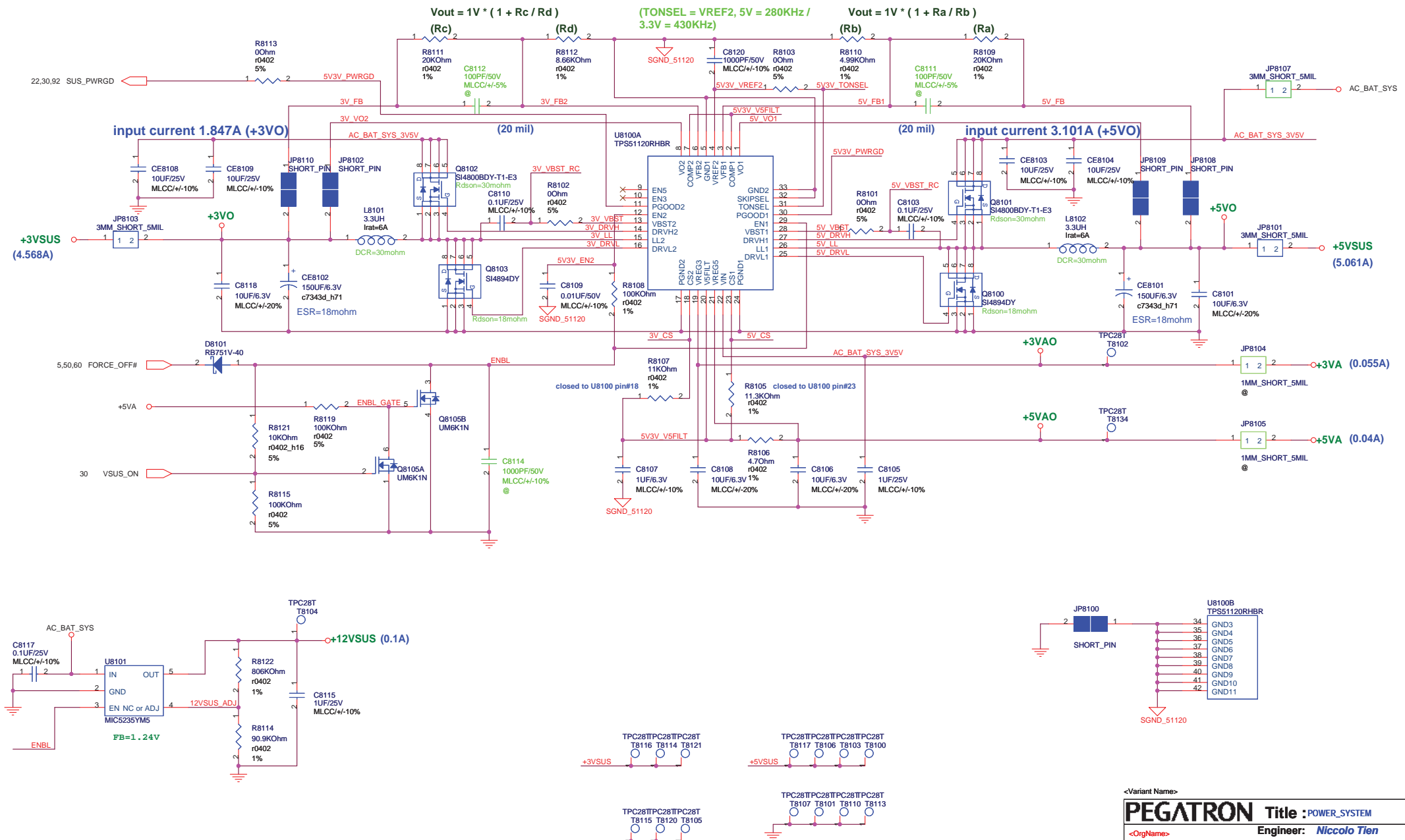
<http://hobi-elektronika.net>

3.3V level logic level: DPRSLPVR, SHDN#  
1.05V level logic: VID, PSI#, DPRSTP#  
 $POUT = (VCSN2 - VGNDs) \times (CSP1 - CNS1 + CSP2 - CSN2) / 16.67mV$

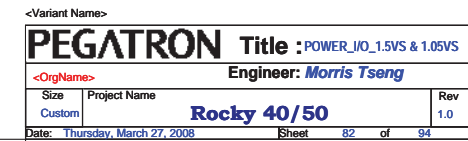




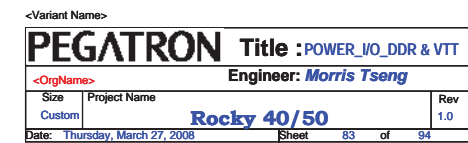
## +5V / +3.3V POWER SUPPLY

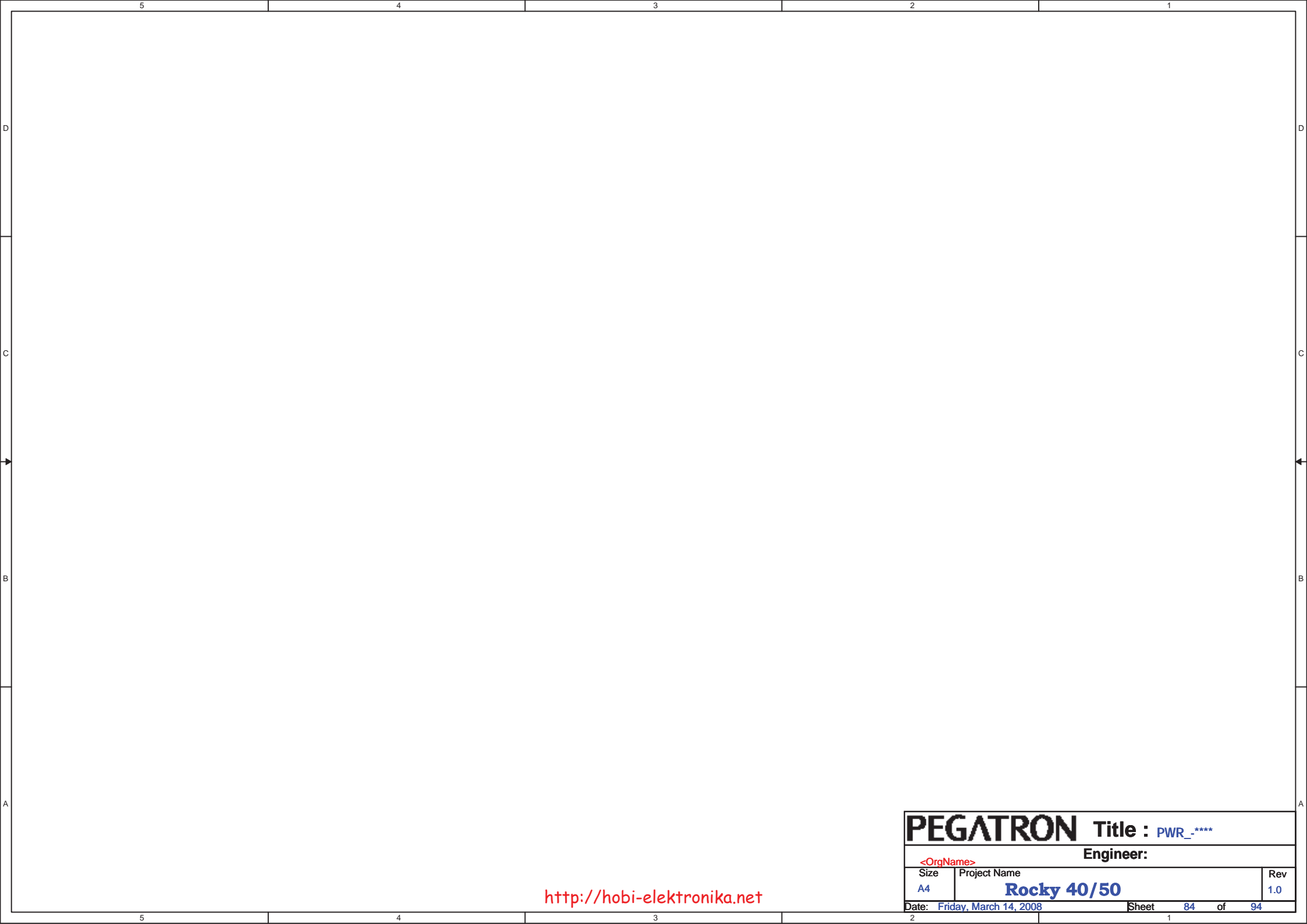


(TONSEL = FLOAT, 1.5V = 360KHz /  
1.05V = 300KHz)



<http://hobi-elektronika.net>





PEGATRON

Title : PWR\_\*\*\*\*

Engineer:

<OrgName>

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date:	Friday, March 14, 2008	Sheet 84 of 94



D

D

C

C

B

B

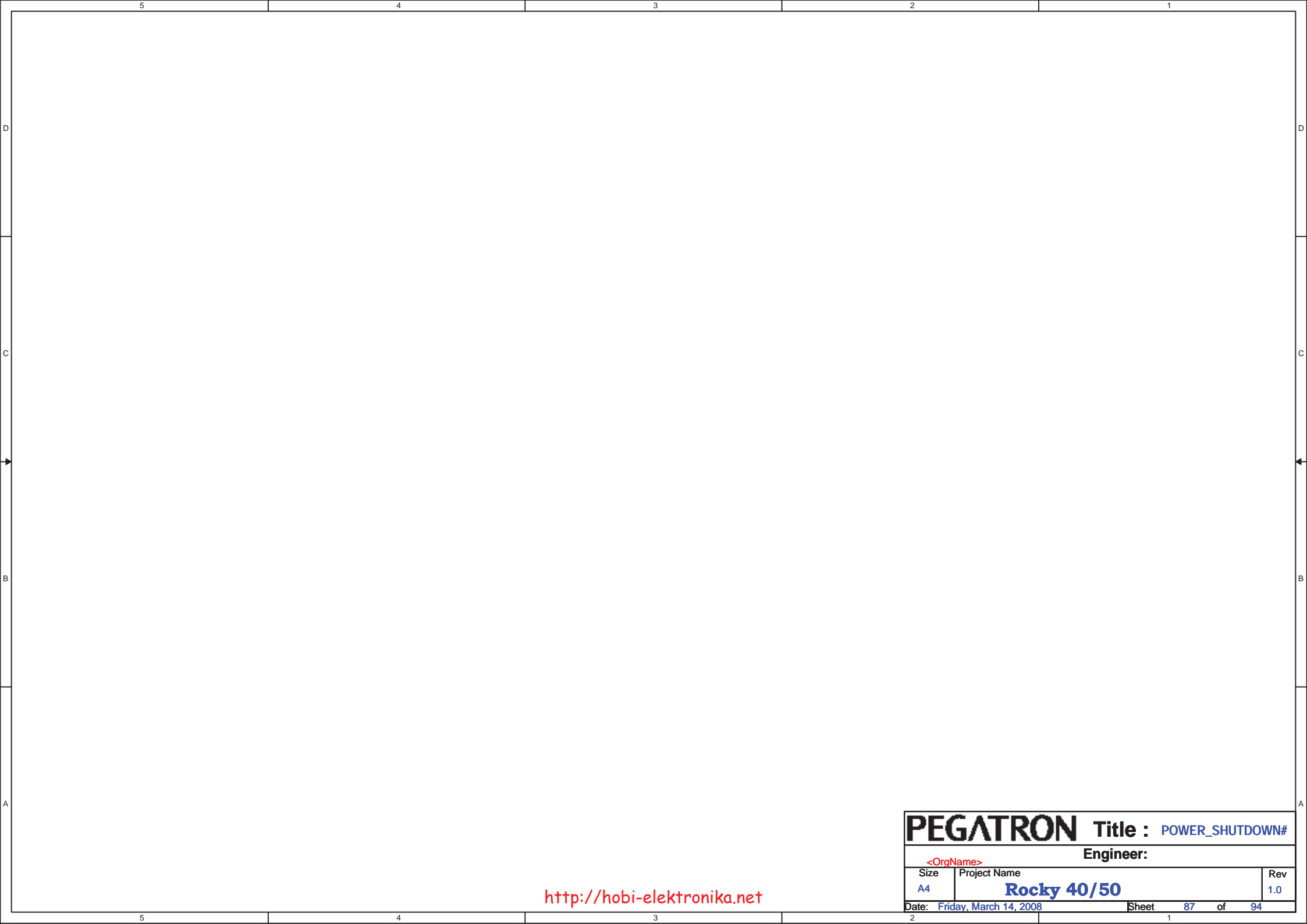
A

A

<b>PEGATRON</b>			<b>Title :</b>		
<OrigName>			<b>Engineer:</b> <i>Niccolo Tien</i>		
Size	Project Name				Rev
Custom	<b>Rocky 40/50</b>				1.0
Date: Friday, March 14, 2008		Sheet		85	of 94

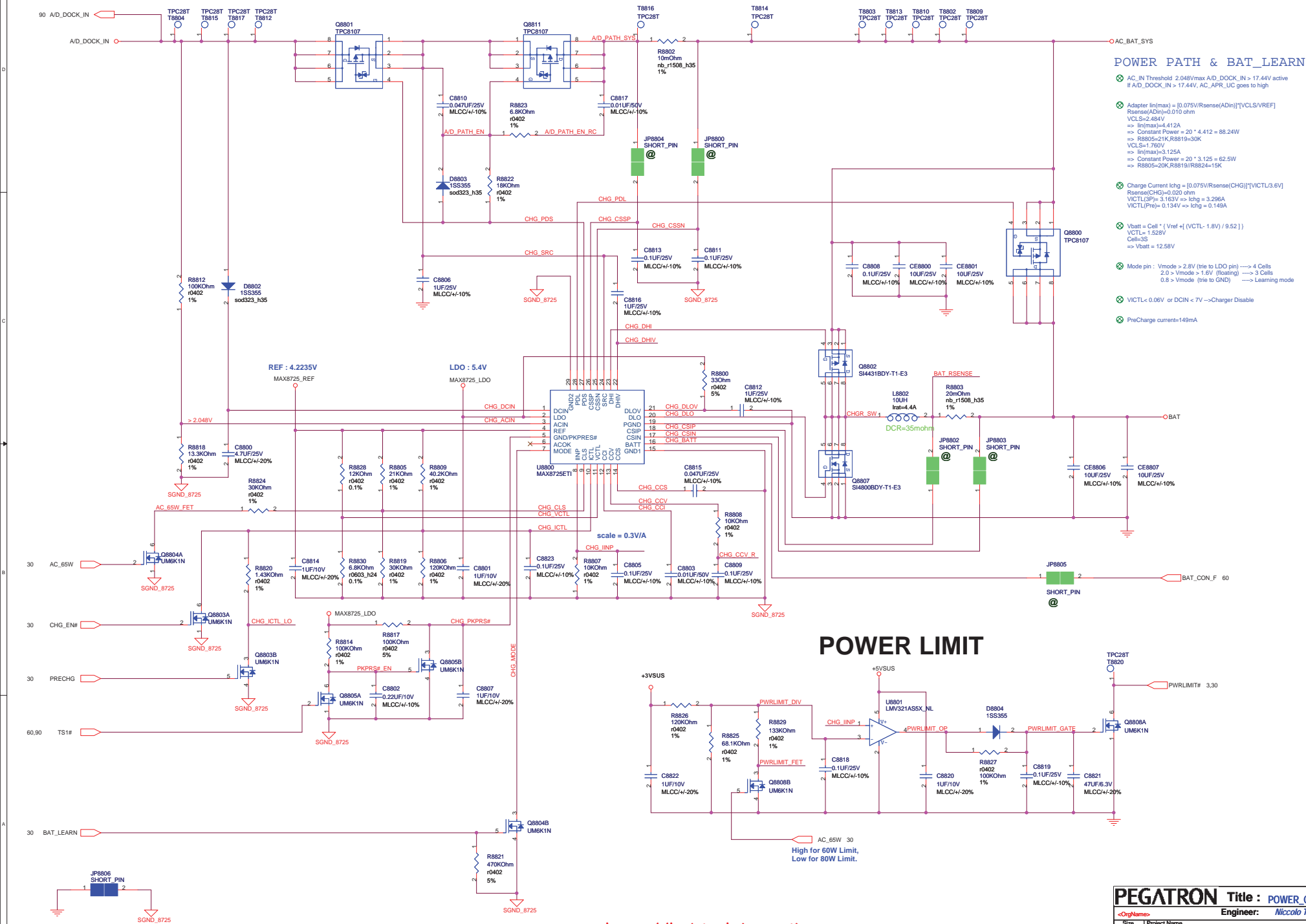
5	4	3	2	1
D				
C				
B				
A				

<b>PEGATRON</b>		Title : <b>PWR_-****</b>	
<OrgName>		Engineer: <b>Niccolo Tien</b>	
Size <b>A4</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>		Sheet <b>86</b>	of <b>94</b>

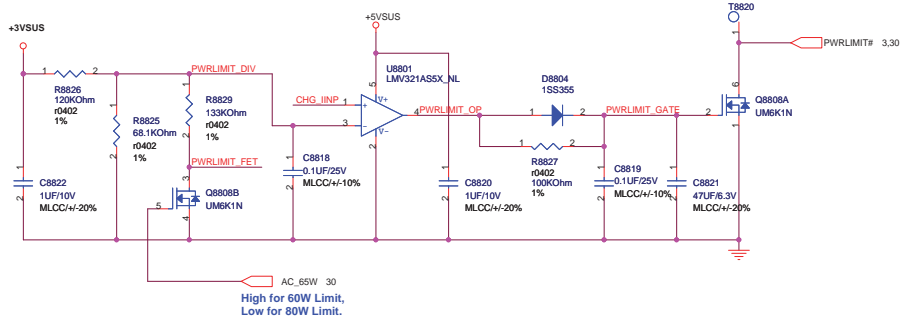


PEGATRON		Title : POWER_SHUTDOWN#	
		Engineer:	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date:	Friday, March 14, 2008	Sheet	87 of 94

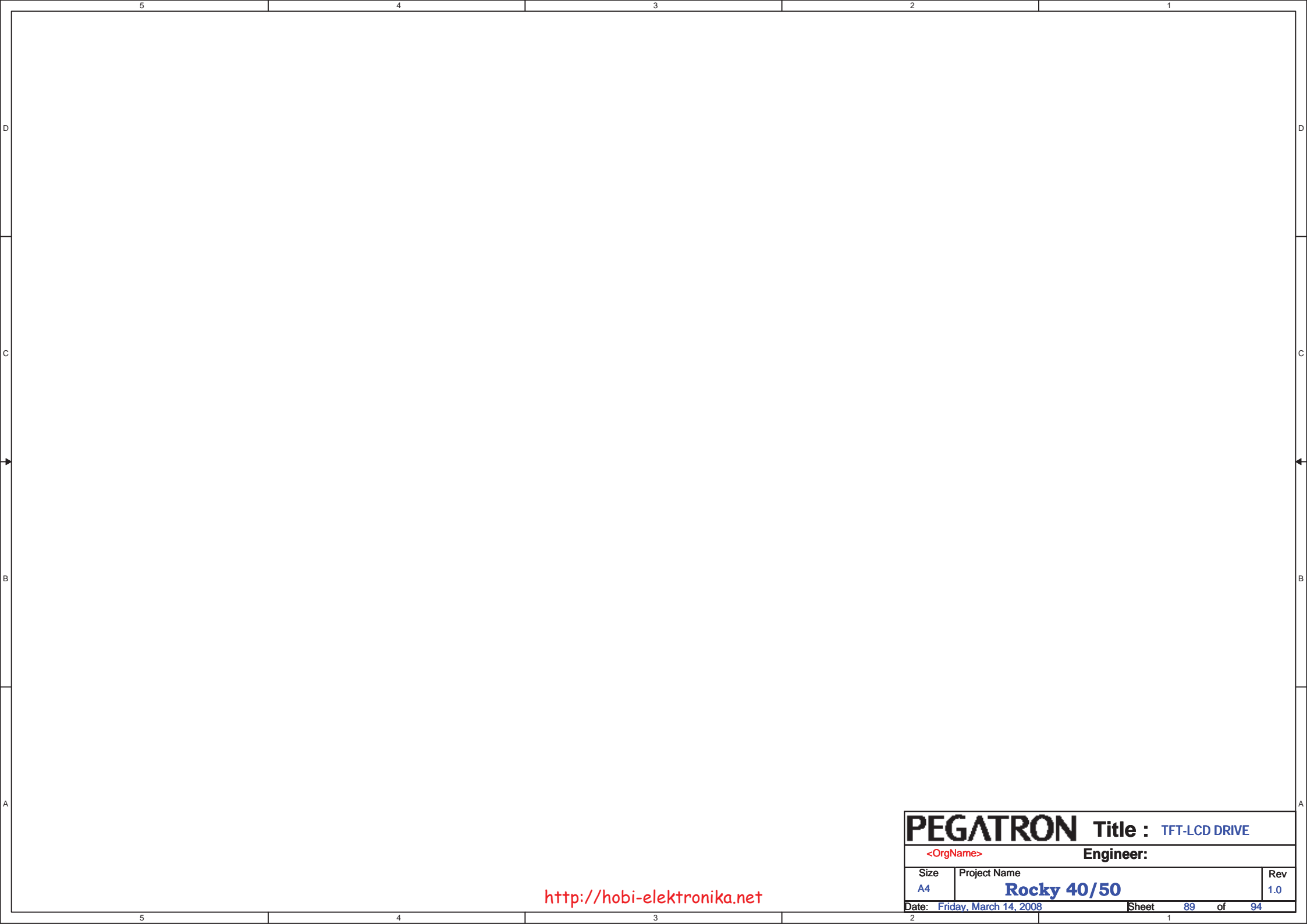
## BATTERY CHARGER



## POWER LIMIT

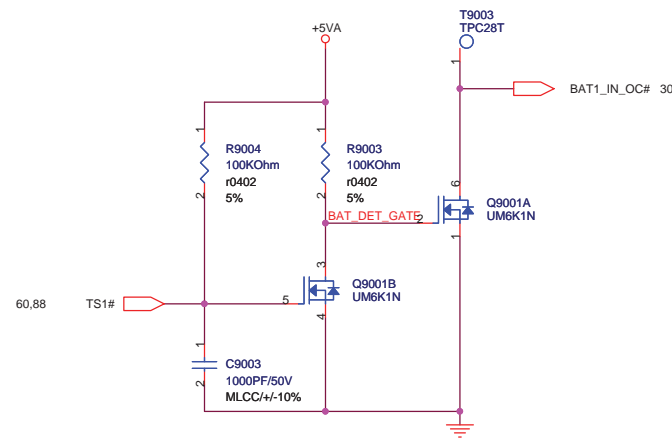




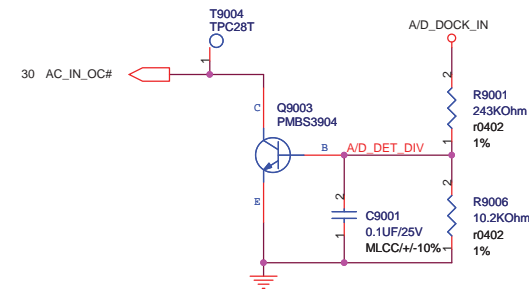


<b>PEGATRON</b>		<b>Title :</b> TFT-LCD DRIVE	
<OrgName>		<b>Engineer:</b>	
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008		Sheet	89 of 94

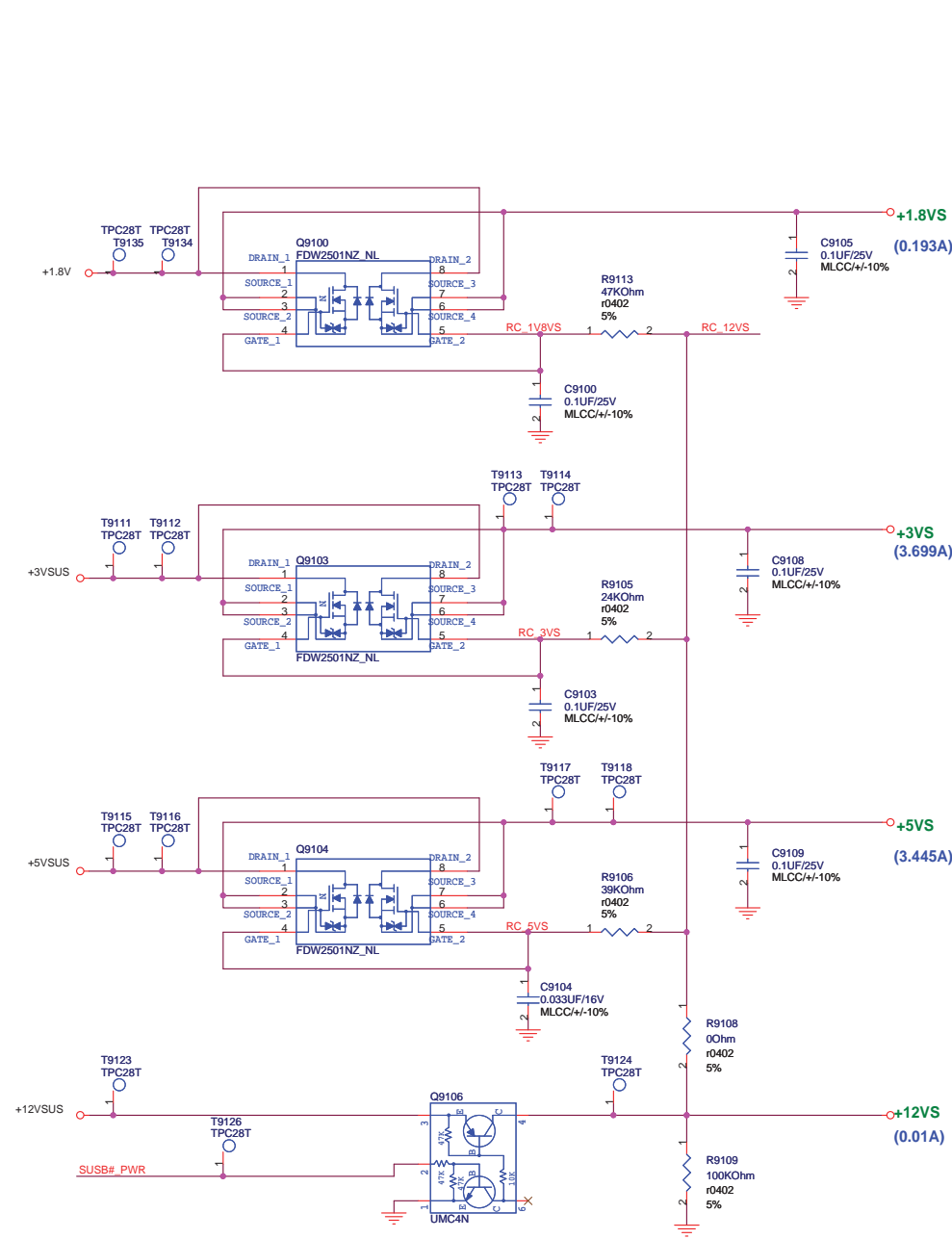
## BATTERY IN DETECT



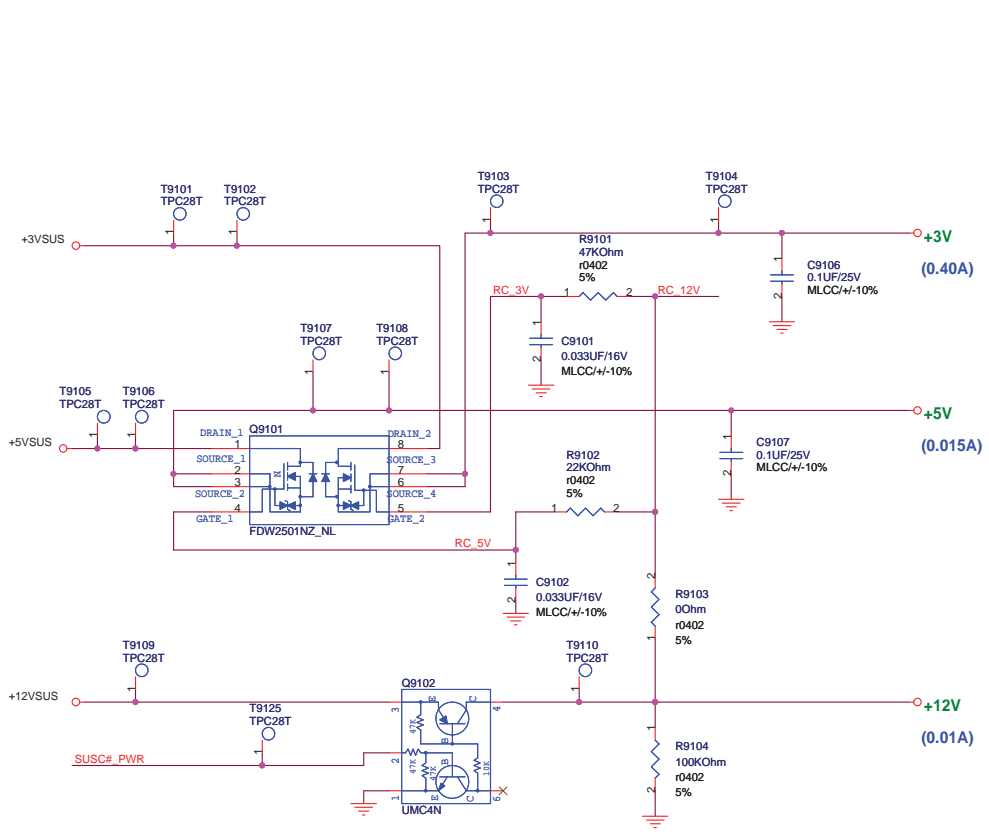
## ADAPTER IN DETECT



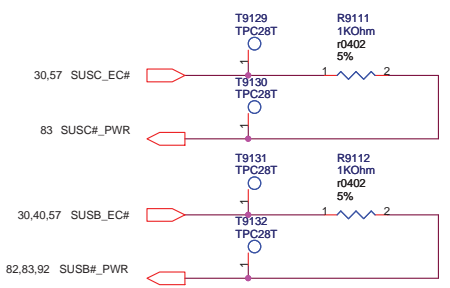
SUSB#\_PWR Load SW



SUSC#\_PWR Load SW



Enable Signal



# POWER GOOD DETECTOR

